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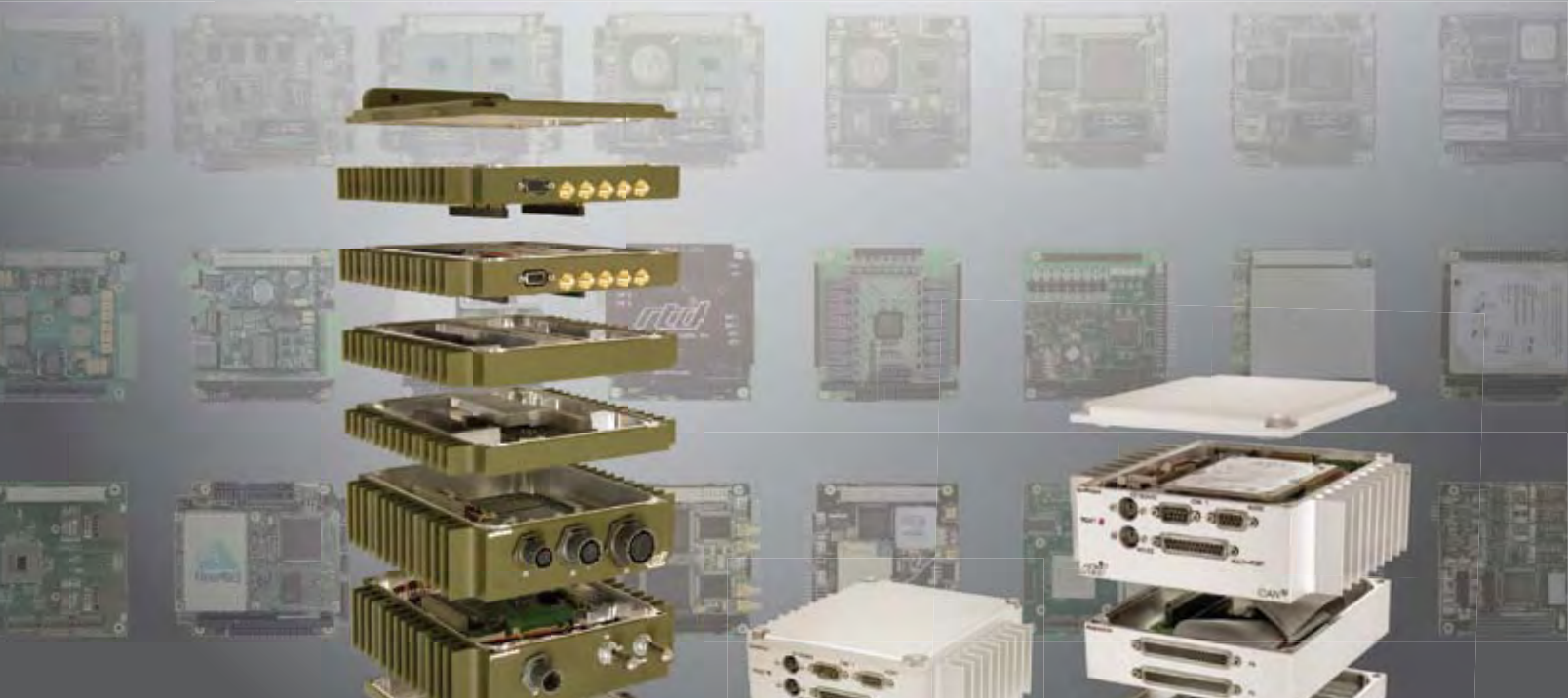
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12 Pre-Integrated Systems Move Up the Solution Food Chain

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COTS (kots), *n.* 1. Commercial off-the-shelf. Terminology popularized in 1994 within U.S. DoD by SECDEF Wm. Perry's "Perry Memo" that changed military industry purchasing and design guidelines, making Mil-Specs acceptable only by waiver. COTS is generally defined for technology, goods and services as: a) using commercial business practices and specifications, b) not developed under government funding, c) offered for sale to the general market, d) still must meet the program ORD. 2. Commercial business practices include the accepted practice of customer-paid minor modification to standard COTS products to meet the customer's unique requirements.

—Ant. When applied to the procurement of electronics for the U.S. Military, COTS is a procurement philosophy and does not imply commercial, office environment or any other durability grade. *E.g., rad-hard components designed and offered for sale to the general market are COTS if they were developed by the company and not under government funding.*

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Coming in August
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On The Cover: Space shuttle Atlantis lifts off from Launch Pad 39A at NASA's Kennedy Space Center in Florida on the STS-132 mission to the International Space Station on time at 2:20 p.m. EDT May 14, 2010. The mission marks the final flight of Atlantis and the first of the shuttles to be retired as the shuttle program moves toward its scheduled termination this year. (NASA Photo)



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PRESIDENT

John Reardon, johnr@rtcgroup.com

PUBLISHER

Pete Yeatman, mail@yeatmangroup.com

Editorial

EDITOR-IN-CHIEF

Jeff Child, jeffc@rtcgroup.com

CONTRIBUTING EDITOR

David Cotton, davidc@rtcgroup.com

MANAGING EDITOR

Marina Tringali, marinat@rtcgroup.com

COPY EDITOR

Rochelle Cohn

Art/Production

CREATIVE DIRECTOR

Jason Van Dorn, jasonv@rtcgroup.com

ART DIRECTOR

Kirsten Wyatt, kirstenw@rtcgroup.com

GRAPHIC DESIGNER

Christopher Saucier, chriss@rtcgroup.com

GRAPHIC DESIGNER

Maream Milik, mareamm@rtcgroup.com

WEB DEVELOPER

Hari Nayer, harin@rtcgroup.com

Advertising

WESTERN REGIONAL SALES MANAGER

Stacy Mannik, stacym@rtcgroup.com
(949) 226-2024

WESTERN REGIONAL SALES MANAGER

Lauren Trudeau, laurent@rtcgroup.com
(949) 226-2014

EASTERN REGIONAL SALES MANAGER

Shandi Ricciotti, shandir@rtcgroup.com
(949) 573-7660

ASIAN REGIONAL SALES MANAGER

Jessica Marinescu, jessicam@rtcgroup.com
(+852) 2548 5100

BILLING

Cindy Muir, cmuir@rtcgroup.com
(949) 226-2000

COTS Journal

HOME OFFICE

The RTC Group, 905 Calle Amanecer, Suite 250, San Clemente, CA 92673
Phone: (949) 226-2000 Fax: (949) 226-2050, www.rtcgroup.com

EDITORIAL OFFICE

Jeff Child, Editor-in-Chief
20A Northwest Blvd., PMB#137, Nashua, NH 03063
Phone: (603) 429-8301 Fax: (603) 424-8122

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Notebook

This Is Your Life Robert Gates

In 2006 Secretary of Defense Robert Gates rolled onto the scene. For many he was a breath of fresh air following Secretary Donald Rumsfeld. But there were just as many that weren't sure where Mr. Gates would take the military. It didn't take long before he made it clear that he felt his mission was to redirect the military for the types of conflicts they would be needed in for the future and to eliminate much of the effort going into peer to peer mentality. Similar stated efforts by previous Secretaries of Defense were just talk. It made for good discussion around water coolers. As stated here numerous times: changing the Department of Defense is like trying to turn an aircraft carrier with an outboard motor.

Robert Gates must be doing something right because almost every group involved with the military doesn't care for him. But he hasn't experienced a General McChrystal situation...yet. Also, he started out in a Republican administration and he's now in his second year as part of a Democratic administration. Many believed that his sole purpose was to act as the new administration's scapegoat for actions in Iraq and Afghanistan. That may yet come to pass, but it's not on the horizon.

For my part, I've made numerous statements saying that he couldn't do it. But now I must confess I think he actually is starting to turn the aircraft carrier. We're seeing signs that at least the uniformed services are changing to be more in line with Gates. Congress on the other hand is still Congress. His way of dealing with some of the "stuff" Congress sticks into the DoD Budget for their political betterment is to just plain keep anyone from signing off on it. It's like a pocket veto, and with elections coming up, Congress just isn't sure how to deal with Gates. As long as the SecDef works within the framework of a fluid military administration policy, he remains highly useful to them. Since Gates' support from the very beginning was a situation of convenience for all entities involved, you can bet that when he is no longer SecDef everyone will turn on him. Silently he will become one of the unsung heroes—like Secretary of Defense William Perry, who managed to break the back of a military philosophy that could have destroyed the defense of our nation. I'm forever grateful to Dr. Perry for his support in bringing *COTS Journal* to life and speaking at *COTS Journal's* coming-out party twelve years ago. Maybe we can get Robert Gates to speak at *COTS Journal's* 20th anniversary.

Now that the aircraft carrier is just starting to turn, tough decisions have to be made and funded. More importantly, RDT&E (Research Development Test & Evaluation) funds have to be allocated in order to develop the needs of this new military. Talking to people in the military embedded industry, RDT&E funds are as

scarce right now as water in the Sahara. Yes, embedded deliveries for 2010 will still have growth over last year, but these are all funded and scheduled programs. With system and pre-integrated systems product development to deployment times still taking years, any long-term gap like we've experienced for the last six months will create difficult times for the military as well as for the embedded industry. Since many of the suppliers of embedded products to the military also have a commercial element—which has been in the dumps for the last few years—interruption of RDT&E funds will produce some casualties among suppliers.

RDT&E for the "new" military may not be the final element necessary for Gates to feel he's completed his mission in establishing and implementing a future direction for the military. But it may be the straw that breaks the camel's back. The "new" military cannot continue to transition on rehashed "old" military products, and the end-all to everything military is not UAVs. So Gates may be in for the perfect storm: an administration that is already not pleasing the doves (nor the hawks), a Congress that's feeling thwarted, and a military that isn't happy that someone other than them is trying to change the rules of their club.

Prime military contractors have already started to hunker down and feed on the bones of some smaller companies that aren't in the position to weather these cyclical dips in release of funds from the military budget. Almost two decades ago we had a similar cycle. Many companies swore they would get out of the military market, only to find that there was no free lunch in the non-military market. Those that hung on until it was over were in a good position to capitalize on the change and owe their growth to the military market.

Primes and sub-tier primes are all holding on to the core of their system product development teams waiting for the inevitable release of funds. That means that military embedded suppliers need to work what is available to them now. There are many opportunities to push "no charge" evaluation items. They need to find the funds to have their sales and marketing staff in face-to-face contact with potential program teams, work co-op deals, be creative and stay around. Secretary Gates may not be around. He will more than likely submit his resignation this year. Aside from the fact that the stress of this position is monumental, he may feel that there isn't much more he can do—or maybe his ouster may suit the politicians. ■■

A handwritten signature in black ink, appearing to read "Pete Yeatman".

Pete Yeatman, Publisher
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The Inside Track

Rochester Electronics Ramps Up Anti-Counterfeiting Efforts

Rochester Electronics is stepping up its efforts to lead the semiconductor industry in the fight against counterfeit and substandard parts, which are increasingly causing both economic and life-threatening havoc worldwide. Part of that effort is to provide only products and services that are 100% authorized by original manufacturers, 100% guaranteed and 100% traceable (Figure 1). In addition, Rochester has worked with industry and government agencies; published authorized distributor source information; and instituted awareness programs. In furthering the fight against counterfeiting, Rochester has aligned with the Semiconductor Industry Association (SIA) and the National Electronic Distributors Association (NEDA). Rochester is also proud to have been classified as a Chinese Reliable Electronic Component Supplier (RECS) by China's Ministry of Industry, a program jointly administered by the China Electronic Purchasing Association (CEPA) and the China Quality Association for the Electronics Industry (CQAE).

As a member of the SIA Anti-Counterfeit Task Force, Rochester



Figure 1

COTS Journal's Jeff Child meets with Rochester Electronics President Paul Gerrish at their wafer fab and test facility.

Electronics has long been a leader in the fight against substandard and counterfeit semiconductors. Rochester, in 2006, held a symposium that broadened awareness and inspired solutions. Attendees included original manufacturers and customers as well as representatives of government and law enforcement agencies. Rochester partners with the SIA to produce the Electronic Authorized Source Directory (www.electronicasds.com), which connects procure-

ment personnel to reputable semiconductor distributors. The directory lists original manufacturers and their authorized semiconductor distributors. Buying only from authorized distributors eliminates the risk of purchasing counterfeit or substandard semiconductors.

Rochester Electronics
Newburyport, MA.
(978) 462-9332.
[www.rocelec.com].

EADS and TTTech Ink Licensing Contract for AFDX

EADS and TTTech Computertechnik AG recently signed a licensing contract for the Avionics Full-Duplex Switched Ethernet (AFDX). This agreement was concluded at the 2010 Berlin Air Show by EADS Chief Technical Officer Jean Botti and TTTech's executives. AFDX is a standardized high-quality data network that provides guaranteed bandwidth and secure communications. AFDX was developed by the EADS Group's

Airbus company, and utilizes a special protocol to provide deterministic timing and redundancy management in the inter-system network environment. This standard first flew on Airbus' A380 jetliner, and has since been applied to a variety of aircraft.

AFDX borrows concepts from the Asynchronous Transfer Mode (ATM) in order to overcome some of the weaknesses of Ethernet. A key feature of AFDX is its Virtual Links (VL) capability. In one abstraction, it is possible to visualize the VLs as an ARINC 429 style network each

with one source and one or more destinations. Virtual Links are unidirectional logic path from the source end-system to all of the destination end-systems. Unlike that of a traditional Ethernet switch, which switches frames based on the Ethernet destination or MAC address, AFDX routes packets using a Virtual Link ID.

TTTech Computertechnik AG
Vienna, Austria
+43 1 585 34 34-899.
[www.tttech.com].

Northrop Grumman Taps Mercury for Radar Processing in Navy BAMS UAV

Mercury Computer Systems announced it was selected by Northrop Grumman to deliver its scalable multicompiling products and services for the U.S. Navy Broad Area Maritime Surveillance (BAMS) Program. Mercury will provide PowerStream 7000 multicompilers, the most powerful embedded computing platform in deployment, and a heterogeneous operating system for the BAMS UAV to enable the processing of synthetic aperture radar (SAR) images. The BAMS UAV is designed to support a variety of all-weather maritime ISR (intelligence, surveillance and reconnaissance) missions. Mercury's PowerStream multicompilers—deployed on some of the world's largest radar platforms—combine FPGA processors with massive I/O and real-time reconfiguration.



Figure 2

A modified Global Hawk, the BAMS UAV is designed to support a variety of all-weather maritime ISR missions.

Northrop Grumman was awarded a contract for the U.S. Navy's BAMS program in 2008. BAMS UAV uses a maritime derivative of the RQ-4 Global Hawk equipped with a 360 degree Multi-Function Active Sensor (MFAS) active electronically scanned array along with Navy-specific ground stations. The BAMS UAV, at full opera-

tional capability, will provides persistence over large maritime distances for long periods of time for up to five simultaneous orbits worldwide.

Mercury Computer Systems
Chelmsford, MA.
(978) 967-1401.
[www.mc.com].

Army Contracts Thales-RaytheonSystems to Modernize AN/MPQ-64 Sentinel Radars

ThalesRaytheonSystems has been awarded a \$21.8 million contract by the U.S. Army to upgrade multiple AN/MPQ-64 Sentinel air defense radar systems. This award is an option to the existing upgrade contract originally awarded in June 2007. The contract will upgrade the U.S. Army Sentinel radar transmitters, receivers and excitors, and increase functional capabilities such as faster data processing and greater detection range for smaller targets. Additional capabilities will also help minimize instances of fratricide



Figure 3
AN/MPQ-64 Sentinel radar is the premier air surveillance and target acquisition and tracking sensor for the U.S. Army's Cruise Missile Defense Systems program.

and accidental counter-missile firing and facilitate a transition to defense-force mobility. Upgrade work will be performed in El Paso, Texas and Fullerton, Calif.

The Sentinel radar is the premier air surveillance and target acquisition and tracking sensor for the U.S. Army's Cruise Missile Defense Systems program. The radar's primary mission is to protect maneuver forces and critical assets from cruise missile, unmanned aerial vehicles and rotary- and fixed-wing threats. The Sentinel accurately acquires targets far enough forward of friendly troops to provide sufficient reaction time for air defense weapons to engage at optimum ranges. More than 200 Sentinel radars are currently deployed by military forces worldwide. Formed nine years ago, ThalesRaytheonSystems is equally owned by Raytheon and Thales.

Raytheon
Waltham, MA.
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[www.raytheon.com].

TORC Products Integrated for Marine Corps UGVs

TORC, a provider of modular unmanned systems technology, provided its full line of Robotic Building Blocks for Virginia Tech engineering students to rapidly develop four optionally unmanned, autonomous vehicles. TORC products make up the key components of the autonomous vehicle kits that were installed on existing platforms to create the four Ground Unmanned Support Surrogate (GUSS) systems.

TORC's ByWire, SafeStop and PowerHub modules were used in the conversion of the base vehicle to provide the drive-by-wire, wireless emergency stop and power distribution systems. Utilizing existing algorithms

developed under previous TORC/VT partnerships such as the DARPA Urban Challenge, a customized version of the AutoNav (autonomous navigation system) was used to provide the advanced off-road tactical behaviors required to meet the needs of the Marine Corps Warfighting Lab. The WaySight (a handheld operator control unit) is used as the primary operator interface for the GUSS vehicles.

TORC Technologies
Blacksburg, VA.
(540) 443-9262.
[www.torctech.com].

General Dynamics to Upgrade NASA Satellite System Ground Segment

General Dynamics C4 Systems, a business unit of General Dynamics, has been awarded a seven-year contract by the National Aeronautics and Space Administration (NASA) Goddard Space Flight Center for the Space Network Ground Segment Sustainment (SGSS) project. The company will modernize the ground system and network for NASA's Tracking and Data Relay Satellite (TDRS) constellation (Figure 4). The indefinite delivery/indefinite quantity contract has a total potential value of approximately \$642.2 million, including options. The period of performance is from June 21, 2010 through June 20, 2017.

As prime system integrator for the project, General Dynamics will implement a new ground-system architecture that ensures the space network will continue to provide global space-to-ground telecommunications and tracking coverage for low-Earth orbit and near-Earth space flight missions. Particular focus will be given to project integration, testing and operational transition so the new system is implemented without interruption to ongoing operations of the



Figure 4
The Tracking and Data Relay Satellite System (TDRSS) is a network of communications satellites—each called a TDRS—and ground stations used by NASA for space communications.

space network, which supports all NASA scientific and human space flight missions, including the Hubble Space Telescope and the International Space Station.

General Dynamics C4 Systems
Scottsdale, AZ.
(480) 441-3033.
[www.gdc4s.com].

Team Demos Autonomous Helicopter Collision Avoidance System

Piasecki Aircraft Corp. and Carnegie Mellon University have developed and flight demonstrated a navigation/sensor system that enables full-size, autonomous helicopters to fly at low altitude while avoiding obstacles; evaluate and select suitable landing sites in unmapped terrain; and land safely using a self-generated approach path. Autonomous flight at low altitude and landing zone evaluation/selection is an unprecedented feat with a full-size helicopter. This technology has been developed to allow



Figure 5
A Boeing Unmanned Little Bird (ULB) autonomous helicopter was used for the navigation/sensor system demo.

future unmanned helicopters to evacuate wounded soldiers from contaminated or live-fire battlefields and to resupply forward

military bases.

In mid-June, the Piasecki/Carnegie Mellon team flight tested the navigation/sensor

system at The Boeing Company's Rotorcraft Systems facility in Mesa, AZ, using the Unmanned Little Bird helicopter (Figure 5). The Piasecki/Carnegie Mellon sensor package and navigation, mapping and collision avoidance software repeatedly demonstrated the ability to land in cluttered environments. In each case, the navigation/sensor system had to map an unknown area where large and small obstructions limited the possible landing sites—circumstances typical of a military or civilian medical evacuation mission. The demonstration was the culmination of work sponsored by the U.S. Army's Telemedicine and Advanced Technology Research Center (TATRC) through a Small Business Innovation

Research (SBIR) program with Piasecki Aircraft and Carnegie Mellon's Robotics Institute, supplemented with significant additional funding from Piasecki.

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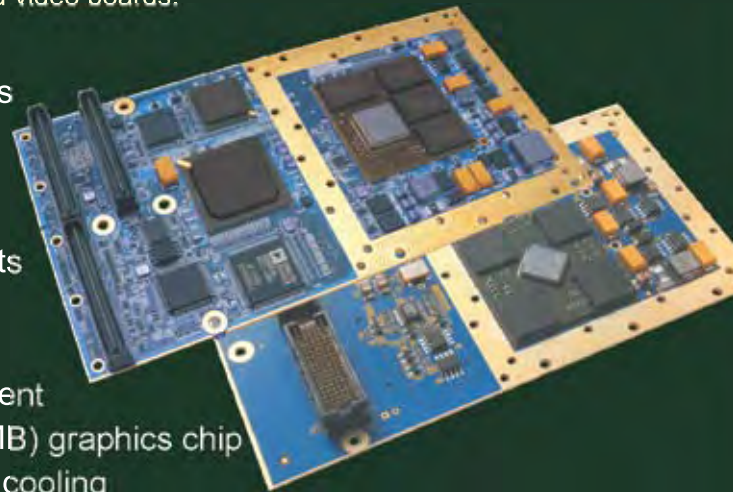
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Pre-Integrated Subsystems

Pre-Integrated Systems Move Up the Solution Food Chain

As pressure to control program costs mounts, the military is on the hunt for new levels of pre-integrated solutions. And embedded computing suppliers are responding.

Jeff Child, Editor-in-Chief



The rising trend toward stand-alone rugged box systems continues to pervade the military embedded computing industry. These box-level systems often resemble the end deliverable systems that prime contractor manufacturers have in the past pieced together themselves using off-the-shelf subsystems. In parallel with the trend toward rugged box-level systems is another trend toward “pre-integrated subsystems.” These are defined as a set of embedded computing and I/O boards put together and delivered as a working system to provide a certain function, but intended to be used in a military customer’s larger system.

Pre-integrated systems usually are made up of a set of modular embedded boards housed in a rugged enclosure that has its own power supply and interface ports to link to a variety of user terminals. This concept of offering a more complete system solution is nothing new. They used to take the form of purely “custom” offerings built from the ground up for specific customers. Today what’s changed is that the concept is now part and parcel of the services many embedded computer suppliers are offering.

Pull from Primes

On the demand side of this trend, prime contractors are shifting to an ever greater reliance on embedded computing suppliers for integration expertise and a level of software development as part of those integration efforts. This is driven by the primes that need to contain their costs—a need that is all the more important as more and more programs are structured as fixed-price rather than cost-plus. New DoD regulations are also helping to fuel the demand for pre-integrated solutions. (The article “New DoD Goals Boost Preconfigured Subsystem Opportunities” by Curtiss-Wright on p.24 of this section explores the impact of those DoD regulations.)

In a recent pre-integrated system design win example, Parvus announced a few months ago that its DuraMAR 1000 routers and DuraNET 2955 Ethernet switches are installed in an Amphibious Assault Vehicle (AAV) (Figure 1) in support of a

SPAWARSYSCEN Atlantic/U.S. Navy technology refresh program to enhance onboard vehicle network-centric capabilities. The units were shipped last year as part of an order through Mercom. Both the legacy Advanced Amphibious Assault Vehicle and its successor, specify a version of Parvus’ DuraMAR IP router subsystem. Parvus also supplies the Tactical Switch Router (TSR) along with several other Line Replaceable Units (LRUs) for the EFV program through a contract with General Dynamics. Both the DuraMAR and the DuraNET 2955 Ethernet switch subsystems are ruggedized versions of COTS Cisco Systems 3230 and 2955 Series products.

Taking On More Integration Duties

Another example exemplifying the shift toward pre-integration was an upgrade program deal won by Mercury Computer Systems last fall. It received a multimillion-dollar system order from a leading defense supplier for its global radar upgrade program. The deal called for Mercury to deliver a complete signal processing solution employing its OpenVPX-compliant Ensemble 6000 Series products. Mercury’s Services and Systems Integration organization meanwhile is providing comprehensive professional services aimed at the development, validation and qualification of the complete subsystem for this ground-based defense system. Mercury’s innovative multi-plane architecture simplified the system design while supporting scalability and facilitating interoperability between the different elements in the system.

Leveraging the design principles of the OpenVPX System Specification, the engineers were able to deliver signal processing capability in a heterogeneous environment overlaid with a systems management infrastructure. According to Didier Thibaud, General Manager of Advanced Computing Solutions at Mercury, the level of integration involvement asked by the customer in this case was significantly more than for the original design, of which Mercury was also the supplier. “In the original design the customer did 75 percent of the integration themselves, and tasked us with 25 percent of the job,” he said. “This time around those numbers were reversed.”



Figure 1

Both the legacy Advanced Amphibious Assault Vehicle and its successor, specify a version of the DuraMAR IP router subsystem, which integrates a Cisco router.



Figure 2

The Vehicle Expansion Unit (VEU) embedded computer system supports integration of multiple applications in a single rugged chassis. It's scalable to up to three independent processors plus video encoding of up to four MPEG channels.

One of the ways suppliers are adding value to pre-integrated systems is to offer systems that have cooling solutions designed in up front. An example is Extreme Engineering's XPand4200 ½ ATR forced air-cooled chassis (reduced height and length) for conduction-cooled modules. This fully ruggedized chassis is designed to meet the rigorous standards of MIL-STD-810 F/G while integrating the latest power-saving and performance-

enhancing technology. The heat from the internal conduction-cooled modules is conducted to sidewall heat exchangers, where it is dissipated to the ambient environment by forced air cooling. Depending on processing requirements, the XPand4200 can be populated with high-performance, low-power, conduction-cooled 3U VPX or cPCI modules designed and manufactured by X-ES. X-ES also has an extensive lineup of conduction-cooled XMC and PMC solutions to fulfill data-processing and I/O requirements. Additionally, X-ES provides integration services for third-party modules.

Application-Specific Systems

Parallel with the trend to pre-integrated solutions is the idea of products tailored specifically to a category of applications—like military vehicles or command and control. Offering a vehicle-specific solution, AP Labs recently announced its newest version of its Vehicle Expansion Unit (VEU) embedded computer system (Figure 2), which provides a rugged, multifunction platform for deploying and consolidating applications within military vehicles used in harsh battlefield environments. The VEU supports efficient integration of multiple applications in a single rugged chassis,

with scalability for up to three independent processors plus video encoding of up to four MPEG channels. Combining independent subsystems within a single thermally efficient fanless chassis provides a compact footprint for optimal Size, Weight and Power (SWaP) and improved maintainability.

At the AUSA Exposition in February, the VEU was demonstrated running Northrop Grumman's NCOMS-P software, providing fact-driven Condition-Based Maintenance (CBM) capabilities for operators/maintainers of military vehicles. The VEU also is used in a battlefield vehicle application that processes multiple video streams from externally mounted camera systems, thereby providing 360 degree observation in real time, even while traveling over rough terrain.

ATCA for Command and Control

Focusing on Command and Control applications, RadiSys brings ATCA into the pre-integrated system military space with its Promentum C2 Server. As the military continues to expand its network-centric warfare capabilities and integrate more platforms together, there is an increased need for mobile computing and communications infrastructure that can be quickly deployed in the field. This portable ATCA platform is designed to provide the performance and features required for rugged, ground mobile applications in the Mil/Aero industry. The C2 Server leverages LCR Electronics' ruggedized ATCA chassis and Astute Networks' Edge Storage Blades in a rapidly deployable, higher performance platform with a more than 30 percent weight decrease and lower power consumption than current Rack Mount Servers (RMS). The C2 Server has been designed to meet the demanding environment requirements of MIL-STD-810 and can quickly be deployed and serviced in the field.

A handful of embedded computing vendors are even making the pre-integrated system idea part of specific platform service and integration initiatives. An example along those lines is Themis Computer's Mission & Payload System Initiative. The concept is to supply kinetic and thermal management technologies



Figure 3

The Mission & Payload System Initiative suite includes an 8-slot, 1/2 ATR high-power chassis with multiple cooling and storage options.

and both shortened lead times and reductions in unit price and overall program cost. Themis demonstration systems in this initiative include preconfigured versions of the 3U VPX and mezzanine modules, backplanes, I/O controllers, front panels and chassis cooling options. These systems allow customers to buy true COTS systems, with a standardized option set, suitable for many Mission Computer, Display Processor, Digital Map, EW Controller, SIGINT Recorder, Bus Data and Voice Recorder, and Payload Management applications.

The initial conduction-cooled 3U VPX MPSI product suite includes a high-performance Intel Core i7 (Arrandale)-based SBC, an AMD E4690-based GPU module, an 8-Port SATA/SAS RAID Controller and XMC/PMC Carrier module and a Mass Storage Carrier for 256 Gbyte flash or 500 Gbyte non-rugged rotating media. I/O options are extended, through the use of the XMC/PMC I/O Carrier, which hosts a wide range of I/O controllers, including MIL-STD-1553, ARINC 429, High Speed Serial, ATDS, Discrete and Analog I/O. Included in the MPSI suite is a series of third-party Software Defined Radio and FPGA Modules. Packaging options for the MPSI suite include two new Themis designed chassis systems, an 8-slot, 1/2 ATR high-power chassis with multiple cooling and storage options (Figure 3); and a 5-slot convection-cooled chassis intended for smaller footprint and lower power applications. ■■

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Pre-integrated subsystems are quickly becoming the go-to solution for many military retrofit or upgrade programs as these subsystems are increasingly turnkey.

Adam Thompson, Application Engineer
Mike Southworth, Marketing Director
Parvus

To meet burgeoning demand, developers of off-the-shelf rugged computing platforms are including a variety of features and services to enhance usability, reduce complexity and increase subsystem durability. Perhaps the most important feature of a pre-integrated subsystem is its ability to perform in a variety of harsh environmental conditions. To meet these rugged requirements necessitated by military deployment, pre-integrated subsystems are often tested and qualified to meet military standards to provide application assurance and reduce the customer's engineering costs. However, buyers need to be cognizant of the differences in the levels of testing and qualifications in today's COTS subsystems.

Qualifying for Military Standards

Some suppliers may describe their products as "designed to meet" military standards, yet they have not performed formal validation testing to prove as much. This simply means that the manufacturer took certain military standards under consideration in the design phase, but appropriate testing has not been conducted yet to certify compliance. Buyers



Figure 1

This pre-integrated DuraCOR system made use of application engineering services to reduce development time.

need to ensure that the system they are investigating for purchase has not only been designed but also "qualified" to meet military standards.

By purchasing a qualified system, customers typically sidestep the additional time, manpower and expense required to pass these stringent military standards. Case in point, if a systems integrator were

to shepherd a device through qualification testing on their own to meet even the basic set of environmental tests for temperature, shock and vibration under MIL-STD-810G, they would not only incur direct lab fees of \$10-20K minimum, but also the resource overhead of preparing the qualification test plans, reports, fixtures, software and cables.

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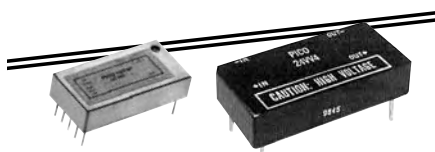


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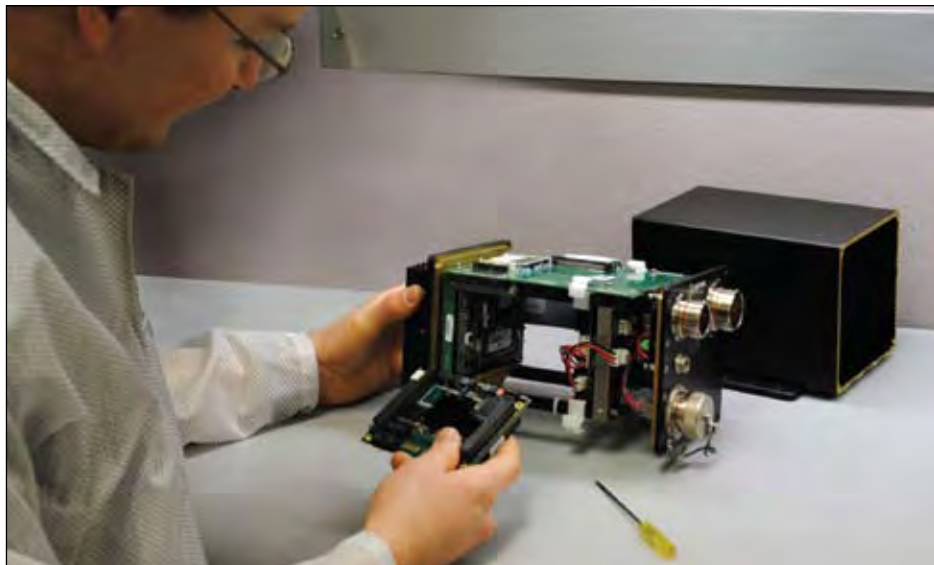


Figure 2

A rugged box-level computer subsystem undergoing thermal testing to qualify for MIL-STD-810G.



Figure 3

Production of integrated DuraCOR computer subsystems equipped with application-specific I/O.

This not only adds time to a project schedule but also additional risk, as there is no guarantee that the device will pass without some re-engineering efforts. Similarly, there is demand for these boxes to be prequalified to MIL-STD-461E for electromagnetic interference/compatibility (EMI/EMC) and safe power supply operation (per MIL-STD-1275D/MIL-STD-704E), which could have an additional \$15-\$25K price tag to complete basic

testing and qualifications. By installing a proven solution, however, customers have the peace of mind knowing their system will perform properly without investing in non-recurring engineering fees themselves for testing and qualification procedures.

Some pre-integrated system suppliers that meet MIL-STD-810G's basic battery of tests—such as temperature (Figure 1), shock and vibration—may also have the capabilities to test their systems

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to expanded criteria such as humidity, altitude, fungus, salt fog, explosive decompression, immersion and sand/dust exposure, if the application so requires it. An added benefit is that if such testing is overseen by the manufacturer of the device, who naturally has the most technical familiarity with the device, the test engineers may be able to address potential design concerns at the testing laboratories on the spot through minor design

changes, thus minimizing potential delays and retesting. Although this type of testing will require extra fees, such testing will ultimately ensure that a rugged computing solution can endure the specific environment for its application.

Alternatively, some suppliers, including Parvus, may be able to perform in-house confidence testing and/or leverage a heritage of test results from similar products, subassemblies, statistical analysis tools and

engineering best practices to detail a case for qualification by technical analysis with any number of the 20 or more test methods included in the MIL-STD-810G standard (Figure 1). This analysis could provide the customer with a high degree of confidence that the system will meet these other criteria without paying for extra testing.

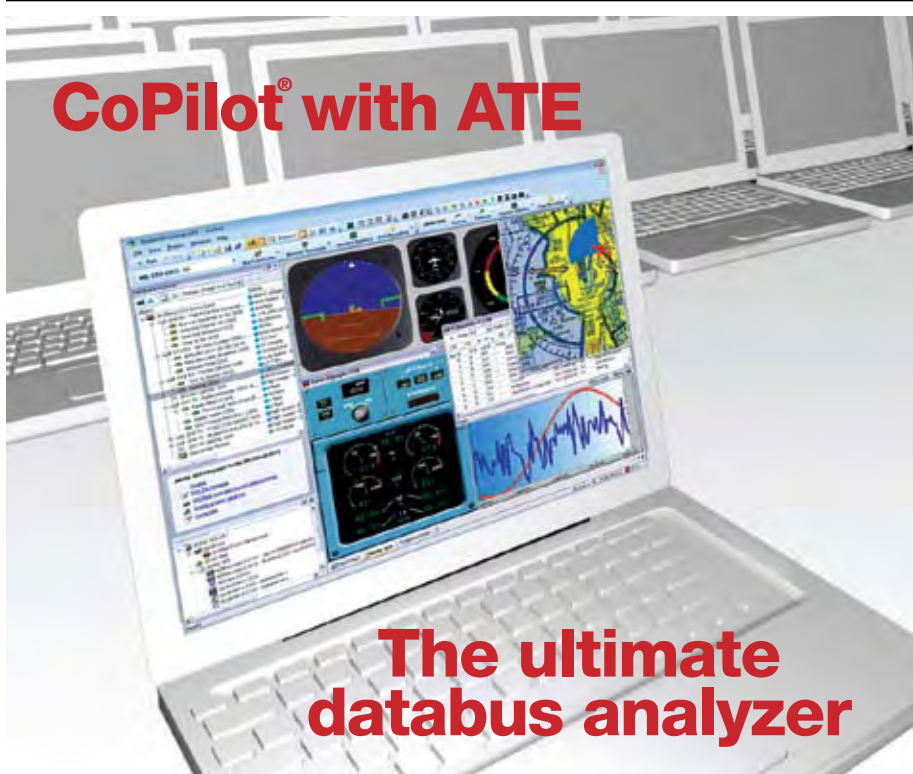
Engineering Turnkey Solutions

As government contracts continue to call out increasing percentages of COTS products, prime systems integrators and their subcontractors alike are rushing to identify “off-the-shelf” solutions that can be implemented across multiple programs. As a result, more and more standard product platform solutions are designed with a considerable capacity for future expansion and flexibility. Many companies, however, are simultaneously facing human resource constraints that restrict their engineering groups from developing next-generation products in house. Application engineering groups at Original Equipment Manufacturers (OEMs) fill this void by assisting system builders with application-optimized, turnkey solutions that reduce development time while increasing customer interface and feedback, ultimately lowering the costs of modifications.

One of Parvus’ customers involved in supplying a ground penetrating radar solution for improvised explosive device detection in the war zones of Iraq and Afghanistan, took advantage of such application engineering services with the DuraCOR 810 mission computer to reduce production overhead and improve efficiencies. The DuraCOR 810 was prequalified to MIL-STD-810 and 461, featured six open PCI04+ card slots, and had a built-in I/O expansion interface to accommodate integration of their add-on cards without mechanical changes (Figure 2). Initially, the customer purchased base DuraCOR 810 subsystems from Parvus and integrated specific third-party I/O cards on their own, along with their application software using their own production resources. This met their needs for about two years while demand was building for their vehicle-mounted mine detection solution.

Pre-Integration at Work

Once demand picked up for their mine sweeping solution, however, the customer



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MIL-STD-1553
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tapped Parvus' application engineering and production services to provide a turnkey system, complete with the integrated third-party cards. As the manufacturer, it was ultimately more efficient and cost-effective to have Parvus integrate the added I/O at time of manufacture, troubleshoot any issues at the factory, perform burn-in testing, do environmental stress screening and deliver a tested solution ready to deploy (Figure 3).

Such an approach eliminated inefficiencies associated with disassembling the platform by the customer to integrate their custom I/O, reassembling it and retesting. Instead, it placed production responsibility with the OEM of the subsystem, which naturally has the most familiarity, best production tools and comprehensive working knowledge of the product's operations. As a result, this has reduced in-field fallout for the customer and is enabling them to experience faster time to deployment and reduced ongoing support costs.

Subsystem integration services, also called application engineering, is becoming increasingly popular as customers witness the cost benefits of leveraging qualified COTS subsystem platforms. Application engineering teams quickly become experts at understanding requirements and proposing the most rugged yet cost-effective approach to meet their program's functional and environmental requirements. Common requests of Parvus application engineers include the integration of application-specific boards, loading of custom operating systems, upgrading of memory/mass storage devices, and handling mechanical, connector or interface customizations.

Engineering I/O Solutions

These services are typically rendered with minimal lead times, yet done in accordance with ISO 9001 quality management processes and best engineering design practice principles. Commonly requested functionality includes the integration of MIL-STD-1553 data bus controllers for communication with avionics or vehicle sensors, and the addition of asynchronous/synchronous serial ports or Ethernet switch ports for situational awareness links to tactical radios, satellite

modems and other onboard equipment. Video capture and encoding and other analog/digital I/O are also common.

Application engineers provide accessibility between design engineers and customers to ensure their integrated subsystem will meet user demands and provide the best deployment possible. Since these engineers often serve as the technical point of contact when optimizing systems, communication between the manufacturer's

resources and the customer is greatly improved. This communication not only ensures that customers' expectations are being met, but also provides valuable market trend information to the teams developing the next-generation products.

Flexibility Is Key

Since many subsystem platforms are based on open-architecture embedded board standards such as PC/104, VPX,



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Figure 4

Northrop Grumman employees conduct maintenance on an MQ-5B Hunter UAV. Its Payload Interface Unit (PIU) is based on a pre-integrated system.

or CompactPCI, customers have a high degree of flexibility in tailoring their subsystem I/O in house or through application engineering groups with minimal re-engineering effort. Some models allow the customer to tailor their device with mission-specific I/O and boot-up-out-of-the-box functionality by including extensive expansion opportunities.

These models include multiple open card slots, as well as expansion connectors

pre-routed to exterior interface boards. These devices are also greatly improved by developers that offer a pre-loaded operating system optimized for the subsystem's basic hardware. The ability for customers to modify their own device is a key motivator for the further adoption of this technology as it reduces costs and speeds time to deployment.

UAV Program Example

Such was the case for Melhcorp, a military subcontractor that designed the Payload Interface Unit (PIU) for the MQ-5B Hunter UAV (Figure 4). Melhcorp was selected by Northrop Grumman to manufacture, maintain and support three different types of payload interface components for the MQ-5B Hunter unmanned aircraft. Melhcorp chose the Parvus DuraCOR 810 for the Hunter program because of its rugged design and modularity. More than 40 DuraCOR 810 subsystems have been delivered to Melhcorp, which they have configured with additional cards to monitor, control and communicate between payloads on board the Hunter.

Pre-integrated subsystems have come of age and are proving themselves as the computing device of choice for demanding military environments. The advances made in COTS technology, combined with a growing set of integration services, will continue to push these computing solutions further into applications where only the most durable, rugged systems will suffice. ■■

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New DoD Goals Boost Preconfigured Subsystem Opportunities

Thanks to changes in DoD policies and budget goal, the focus has shifted toward upgrading existing systems. That's driving a need for complete pre-integrated systems that shrink development cycles and offer working solutions sets.

Mike Macpherson, Director, Business Development
Curtiss-Wright Controls Embedded Computing

Recent changes in the U.S. military's mission strategy—following the change of administrations, and reflected in the DoD's new budget—are shifting the military procurement landscape. One of the changes that promises to significantly impact the embedded COTS market is a reduction in the number of new program starts along with a large increase in the number of programs for upgrading and networking existing systems. All that calls for an associated reduction in the time from development to deployment for new technologies. These new Defense Department procurement policies are helping to drive increased interest in pre-configured subsystems from COTS vendors.

The Weapon Systems Acquisition Reform Act passed by the U.S. Congress and signed by President Obama in 2009, modified the way that the Pentagon contracts and purchases major weapons systems. In an effort to cut military spending and reduce waste, the Act demands more technology demonstration of new technologies. It also pushes for demonstrations earlier in the program development phase, and for the desired technologies to have higher technology readiness levels (TRLs) than previously required or desired.

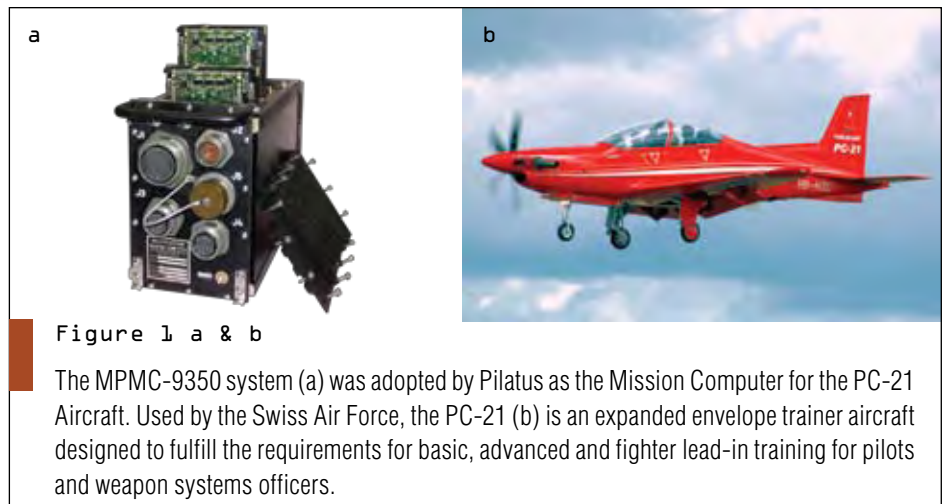


Figure 1 a & b

The MPMC-9350 system (a) was adopted by Pilatus as the Mission Computer for the PC-21 Aircraft. Used by the Swiss Air Force, the PC-21 (b) is an expanded envelope trainer aircraft designed to fulfill the requirements for basic, advanced and fighter lead-in training for pilots and weapon systems officers.

A Focus on Upgrades

The transformation of the Army's acquisition strategy means that instead of developing many new programs, the emphasis will be on upgrades, modifications and evolutionary development. And the selection will be done through technology demonstrations of mature solutions. The new approach seeks more mature technologies sooner to build and support the technology demonstration phase. The demonstration phase is more likely, too, to involve multiple suppliers in an effort to stimulate competition. This trend is helping to make prepackaged and prequalified subsystems of greater inter-

est to platform manufacturers who now find themselves with less time and available DoD funding to develop a desired technology internally.

A related trend is that the DoD is increasingly focusing on capabilities rather than requirements. Prior to the new acquisition reforms, it was more common for system developers to be tasked with application requirements that they would then endeavor to satisfy. Today there has been a shift to emphasize capabilities. In other words, the vendor is asked to demonstrate what capabilities their technology offers. This means that fully integrated, tested and qualified technologies

are the most desired solutions, making it more attractive for military contractors to seek subsystems that have already been deployed and proven.

A Trend toward Solution Sets

In response, COTS vendors such as Curtiss-Wright Controls, are evolving and enhancing their preconfigured subsystem product families, going beyond the traditional “universal machine” approach of offering generic interoperable modular building blocks for the customer to adapt to their application, to instead providing fully defined solution sets. The knowledge and experience obtained building universal “packaged” COTS systems is enabling embedded computer system vendors to optimize the packaging to offer specific solution sets for applications such as mission computing, vehicle control, network ready computing, or sensor processing, that meet the new need for fast turnaround and high TRL levels.

The DoD’s Directive DoD 5000 defines the TRL levels (see sidebar “Nine Levels of Tech Readiness”). Before the acquisition reform took effect, it was typical for system integrators to address program opportunities with low TRL offerings, developing prototypes and testing them in lab environments before testing in actual platforms before deployment. Now the military is demanding technologies that can show higher level TRLs.

In the embedded board market, for example, in the early days of VME and COTS SBCs, 15 years ago or so, an SBC would typically have a TRL of 3 since there was not enough data and experience from the field on its ability to survive and perform. Today, COTS SBC vendors offer boards that would qualify for a much higher rating of 8, following successful deployment of individual boards for many years. This same model is applicable to preconfigured subsystems, as vendors such as Curtiss-Wright now have several years of experience fielding Packaged COTS solutions. Combining proven high TRL SBCs with high TRL subsystems enables COTS vendors to offer solutions that match the new acquisition priorities, with rapid delivery of prequalified off-the-shelf preconfigured subsystems.

Nine Levels of Tech Readiness

Technology Readiness Level	Description
1 Basic principles observed and reported.	Lowest level of technology readiness. Scientific research begins to be translated into applied research and development. Examples might include paper studies of a technology’s basic properties.
2 Technology concept and/or application formulated.	Invention begins. Once basic principles are observed, practical applications can be invented. Applications are speculative and there may be no proof or detailed analysis to support the assumptions. Examples are limited to analytic studies.
3 Analytical and experimental critical function and/or characteristic proof of concept.	Active research and development is initiated. This includes analytical studies and laboratory studies to physically validate analytical predictions of separate elements of the technology. Examples include components that are not yet integrated or representative.
4 Component and/or breadboard validation in laboratory environment.	Basic technological components are integrated to establish that they will work together. This is relatively “low fidelity” compared to the eventual system. Examples include integration of “ad hoc” hardware in the laboratory.
5 Component and/or breadboard validation in relevant environment.	Fidelity of breadboard technology increases significantly. The basic technological components are integrated with reasonably realistic supporting elements so it can be tested in a simulated environment. Examples include “high fidelity” laboratory integration of components.
6 System/subsystem model or prototype demonstration in a relevant environment.	Representative model or prototype system, which is well beyond that of TRL 5, is tested in a relevant environment. Represents a major step up in a technology’s demonstrated readiness. Examples include testing a prototype in a high-fidelity laboratory environment or in simulated operational environment.
7 System prototype demonstration in an operational environment.	Prototype near, or at, planned operational system. Represents a major step up from TRL 6, requiring demonstration of an actual system prototype in an operational environment such as an aircraft, vehicle, or space. Examples include testing the prototype in a test bed aircraft.
8 Actual system completed and qualified through test and demonstration.	Technology has been proven to work in its final form and under expected conditions. In almost all cases, this TRL represents the end of true system development. Examples include developmental test and evaluation of the system in its intended weapon system to determine if it meets design specifications.
9 Actual system proven through successful mission operations.	Actual application of the technology in its final form and under mission conditions, such as those encountered in operational test and evaluation. Examples include using the system under operational mission conditions.

Certification Included

Examples of programs where COTS vendors have successfully delivered such solutions include airborne applications that demanded the absolute minimal space, weight and power (SWaP) and NRE possible. In these programs one example customer used a completely developed solution based on the Curtiss-Wright MPMC-9310 Packaged COTS (PCOTS) subsystem (Figure 1). One user

was particularly interested in the PCOTS solution because the configuration had already passed DO-160 testing for Airborne Equipment.

To take this successful preconfigured subsystem approach to a higher level, from universal solution to specific solution sets, requires optimization of the integration of those specific functions into a complete solution onto which the customer can integrate their application. Because these so-

lution sets will have already been qualified through test and demonstration, they will provide the customer with a high TRL solution (TRL 8) much faster.



Figure 2

Smaller box-level pre-integrated systems like the 3U-sized MPMC-9310 are aimed at applications where size, weight and power (SWaP) are a high priority.

The key to providing an optimal solution set preconfigured subsystem is expertise in SWaP. The ability to solve and address thermal management issues on both the board and system level, and to optimize interfaces and interoperability, will enable COTS vendors to provide the highest performance per cubic inch solutions (SWaP-optimized) (Figure 2). Interoperability is easier to achieve when the vendor is able to offer all the various types of boards required for a specific solution set. Such a highly optimized subsystem reduces the customer's integration risk, providing the best possible "in-box experience" so that they can ensure their own customer the best "out-of-box experience."

The solution set approach delivers the higher order solution increasingly demanded by system integrators responding to the new procurement landscape. Where they may have had nine months to develop a solution in house, starting at the lowest level TRL, now they must frequently demonstrate a high TRL solution in only five months. ■■

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Digital Signal Processing for ISR

DSP Architectures Close the ISR Collection-Analysis Gap

To combat rapidly evolving threats, the DoD is looking toward rapid prototyping of cost-effective, high-performance digital signal processing systems to meet stringent form factor and power constraints and achieve mission objectives.

Dr. James A. DeBardelaben, President and CEO
IvySys Technologies

Today's climate of rapidly evolving asymmetric threats is forcing the U.S. military to quickly adapt in order to maintain tactical situational awareness. However, the traditional dependence on custom, stove-piped digital signal processing (DSP) system implementations consisting of application-specific integrated circuits (ASICs) and application-specific standard products (ASSP) is restricting the agility of U.S. military intelligence, surveillance and reconnaissance (ISR) operations.

To address these limitations and volatile threats, the Department of Defense (DoD) is increasingly funding ISR Quick Reaction Capabilities (QRC). However, this new acquisition model challenges tactical ISR system developers to rapidly prototype cost-effective, high-performance DSP systems, while meeting stringent size, weight and power (SWAP) program requirements.

The ISR Collection-Analysis Gap

Over the past few years, the increased

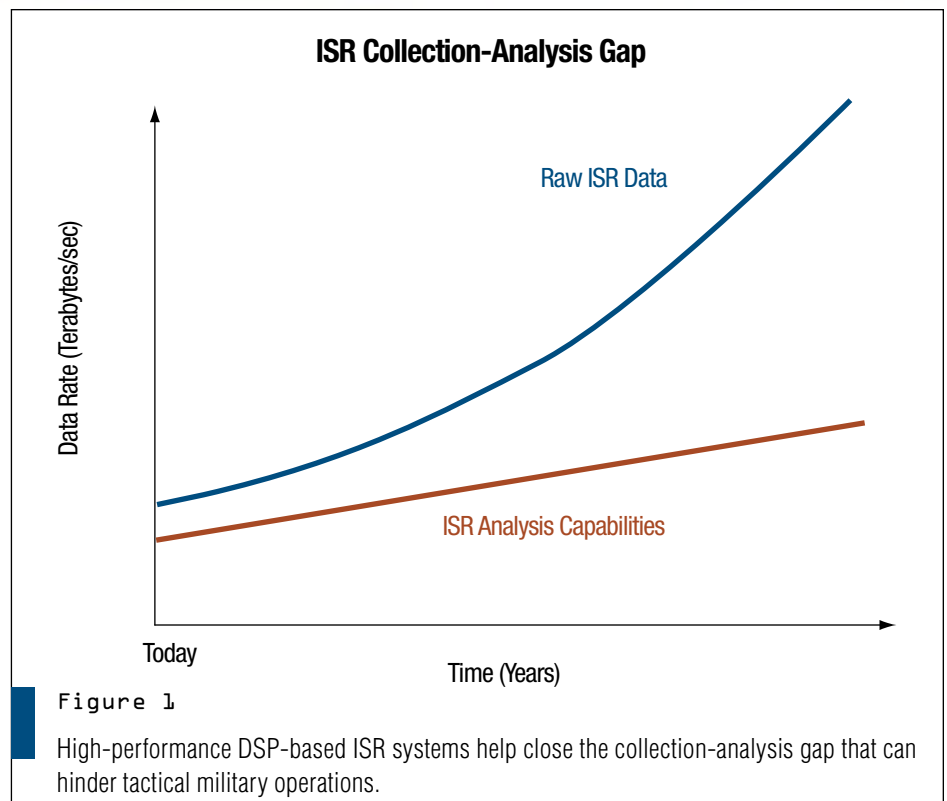


Figure 1

High-performance DSP-based ISR systems help close the collection-analysis gap that can hinder tactical military operations.

demand for ISR capabilities has led to an exponential increase in data collection capacity that shows no signs of slowing in the foreseeable future. However, ISR data processing, exploitation and dissemination (PED) capabilities have only

improved linearly over the same period, leaving a critical gap between collection and analysis capabilities as shown in Figure 1. To close the collection-analysis gap, the DoD needs high-performance DSP-based ISR systems. These systems



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Tilera TILE64 Many-core GPP	ANSI standard C / C++ compiler; profiling and debugging tools for multicore programming; SMP Linux; multicore component libraries for inter-processor core communication	Nominal (Lacks DSP software library support)	1.0	<u>Fixed Point</u> 443 GOPS	<u>Fixed Point</u> 20.1 GOPS/W @22W (all cores active at 700 MHz)
Nvidia Tesla C2050 Many-core GPU	C/C++ /Fortran compiler; cuda-gdb debugger; CUDA Visual Profiler; OpenCL Visual Profiler ; GPU-accelerated BLAS library ; GPU-accelerated FFT library	High (Mature tool and library support for DSP parallel programming)	0.86	<u>Single Precision Float</u> 1.03 TFLOPS <u>Double Precision Float</u> 515 GFLOPS	<u>Single Precision Float</u> 4.2 GFLOPS/W <u>Double Precision Float</u> 2.1 GFLOPS/W @247W TDP
Intel Core i7 -920 Multicore GPP	C/C++/Fortran compiler; Math Kernel Library; integrated performance primitives for multimedia, data processing and communications; threading building blocks; performance analyzers	Very High (Very mature and well integrated tools)	0.72	<u>Single Precision Float</u> 85 GFLOPS	<u>Single Precision Float</u> 0.65 GFLOPS/W @130W TDP
TMS320C6472 Multicore DSP	Code Composer Studio IDE; data visualization kit; math library; signal processing library; image library; floating point emulation	Nominal (Good library support; basic multi-core programming support)	1.0	<u>Fixed Point</u> 256 GMACS <u>Single Precision Float</u> 128 GFLOPS	<u>Fixed Point</u> 47.4 GMACS/W <u>Single Precision Float</u> 23.7 GFLOPS/W @ 5.4W TDP
Altera Stratix V FPGA	Quartus II design software including support for planning, simulation, timing analysis, debugging, verification, and synthesis	Very Low (Time-intensive verification and validation process)	1.24	<u>Fixed Point</u> 1840 GMACS <u>Single Precision Float</u> 1TFLOP	<u>Fixed Point</u> 16.7 GMACS/W <u>Single Precision Float</u> 9.1 GFLOPS/W @110W TDP

Table 1

System developers must optimally trade off the maturity of software tool support with hardware performance and power efficiency to meet high-end ISR application requirements.

DSP ISR Processor Cost and Schedule Implications

Processor	Processor-Specific SW Development Cost Drivers			SAR Processor Cost and Schedule		
	Software Size Adjusted for Reusable SW Availability (Lines of Source Code)	Utilization of Available Execution Time Rating	Execution Time Constraint Effort Multiplier	Processor Board Cost (Approximate)	Software Development Cost Estimate (person-months)	Software Development Time Estimate (months)
Tilera TILE64 Many-core GPP	New: 11000 Reused: 1000	Nominal (< 50% Utilization)	1.0	\$12,000	41.1	12
Nvidia Tesla C2050 Many-core GPU	New: 6000 Reused: 6000	Nominal (< 50% Utilization)	1.0	\$2,500	19.0	9.4
Intel Core i7 -920 Multicore GPP	N/A	Extremely High (> 100% Utilization)	N/A	\$1,500	N/A	N/A
TMS320C6472 Multicore DSP	New: 8000 Reused: 4000	Very High (~ 85% Utilization)	1.31	\$1,500	37.3	11.6

Table 2

The SAR processor case study illustrates the impact that software size, COTS DSP software library support, processor-specific software tool support, and processor throughput constraints have on software development cost and time.

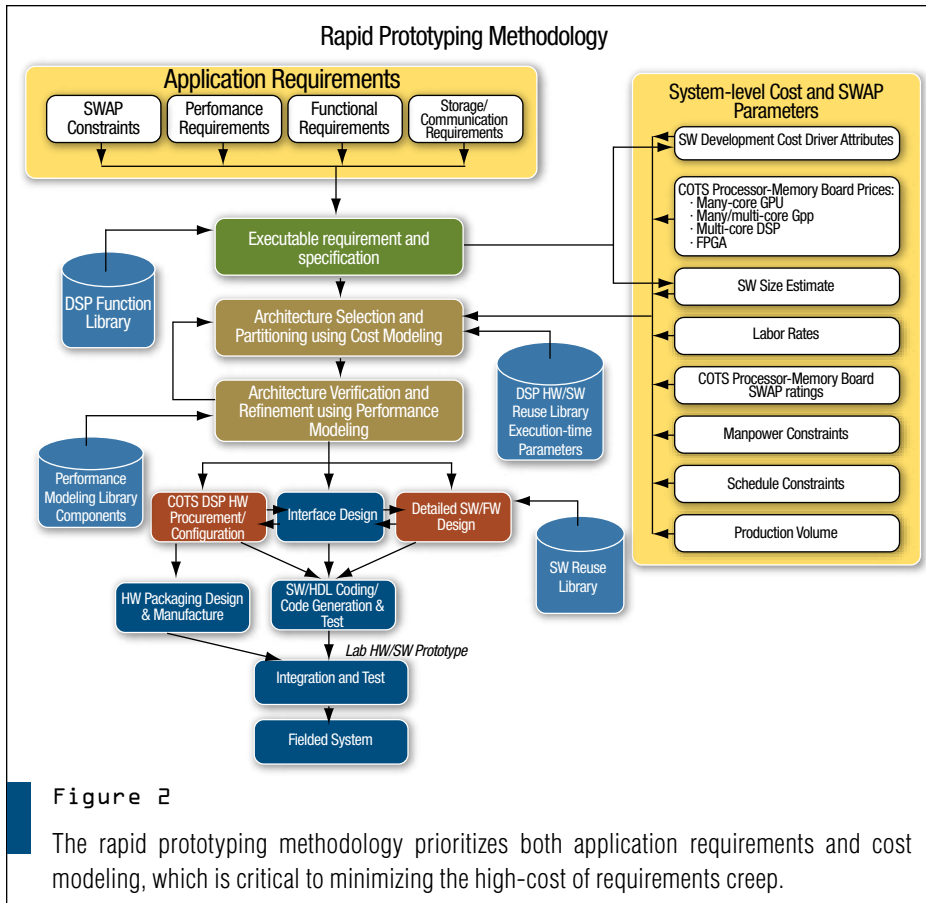


Figure 2

The rapid prototyping methodology prioritizes both application requirements and cost modeling, which is critical to minimizing the high-cost of requirements creep.

enable automated, real-time processing of massive amounts of data and the dissemination of actionable intelligence directly to the warfighter in the field.

High-end ISR applications such as real-time, automated PED push the limits of state-of-the-art DSP technology. Throughput requirements may exceed tens of tera-ops/s. New many-core graphics processing unit (GPU) and general-purpose processor (GPP) architectures are theoretically capable of satisfying high-end performance requirements. It is, however, extremely difficult to develop parallel software algorithms to fully exploit more than only a fraction of the peak performance of many-core architectures.

Many Challenges

The rapid prototyping of cost-effective system implementations that meet extreme performance requirements under severe SWAP constraints is a monumental task. Detailed trade-off analysis and extensive architectural exploration during the architecture selection and par-

tioning stage is critical to accomplishing this goal. Hardware resource slack margins must be optimized to provide maximum performance while minimizing software development cost. Table 1 shows a comparison of many-core GPU, multi/multi-core GPP, multicore DSP and field-programmable gate array (FPGA) with respect to processor-specific software tool availability, processor peak throughput and power efficiency.

Most current ISR systems follow the “waterfall” development method, which dictates a sequential process. The waterfall-type design processes for high-performance ISR systems impose a number of limitations, including: limited architectural exploration; lengthy prototyping times; high cost of design; lack of systematic hardware/software reuse; in-cycle hardware fabrication and testing.

Most design automation activities leverage tool support for detailed system behavioral design, as opposed to early architecture design where much of the system cost is committed. Current indus-

trial practice predominately relies upon designer experience to select system architectures and allocate algorithm functionality. Furthermore, for fully customized ISR systems, hardware and software subsystems are not integrated until after hardware is fabricated, making design errors very costly.

COTS-based Rapid Prototyping

The increased frequency of ISR system development cost overruns and schedule delays has compelled the DoD acquisition community to investigate more effective solutions. The DoD has launched numerous initiatives encouraging contractors to better leverage commercially available DSP hardware boards and system components.

In commercial hardware-based systems, the time and cost of software development can dominate the schedule and budget. One innovative solution garnering attention in the industry is a rapid prototyping methodology. The methodology exploits the use of commercial hardware/software signal processing technologies and software cost modeling, achieving significant reductions in total ISR system cost and development time.

This approach leverages a library-based optimization framework that trades off throughput, hardware/software development costs and schedule, procurement costs and SWAP. The rapid prototyping methodology maximizes system architectural exploration at the front-end of the design process. The resulting solutions are cost-effective DSP embedded systems that exploit the flexibility of many-core GPU, multi/multi-core GPP, multicore DSP and/or FPGA technologies, while satisfying stringent SWAP constraints dictated by mission objectives.

Figure 2 illustrates this rapid DSP system prototyping methodology. The process starts by translating written system requirements into executable requirements and specifications. This is achieved with signal processing libraries and integrated graphical user interface (GUI) toolkits, such as those available in MATLAB. The executable requirements and specifications pro-

vide an early prototype, allowing the customer to validate original requirements and remove ambiguities. The feedback captures any requirement alterations as early as possible, which is critical to minimizing the high cost of requirements creep, one of the most common risks in software projects.

Focus on Costs

After the validation of system requirements, system-level cost parameters, application requirements and performance statistics, these components feed the architecture selection and partitioning optimization process. System developers can use parametric cost models, such as COCOMO II, to drive the architecture trade-off analysis, producing hardware/software architectural candidates that minimize total system cost and development time.

Cost parameters include: software cost driver attributes (size, product, platform, personnel, project), hardware procurement costs, product deployment deadlines, schedule constraints, and labor costs and constraints. Application requirements include SWaP, environmental, precedence and real-time constraints, as well as functional, memory and communication requirements. Performance statistics consist of benchmark time measurements of DSP primitives (such as the fast Fourier transform) executing on the DSP processor boards (for instance, many-core GPU, multi/many-core GPP, multicore DSP, FPGA) contained in the reuse library.

System developers can simulate the resulting architectural candidates using dynamic performance modeling tools to verify that an architecture meets system-level requirements. After performance modeling, the system architect feeds communication overhead parameters such as communication queuing delays and bottlenecks back to the architecture selection stage for refinement. The methodology produces new architecture candidates with the updated model parameters and repeats the process until the architecture meets performance requirements, no longer changing between successive iterations.

The refined hardware/software architectural candidate moves on to the detailed architecture design stage for detailed software and/or firmware design, hardware/software interface design and commercial hardware technology procurement. Depending on the DSP hardware platform and architecture selected, the DSP software and/or firmware design process heavily leverages reusable libraries developed in previous projects.

The cost of assessing, selecting, assimilating and modifying the reusable component must also be minimized to significantly reduce software development cost and time.

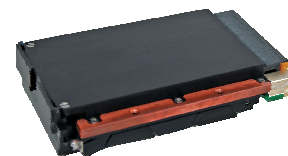
System designers can refine the candidate architecture's Simulink performance model and high-level MATLAB algorithms into Embedded MATLAB code to permit automatic code generation into the C programming language or

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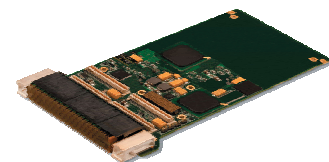
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a hardware description language. To enable the use of automated code generation tools, sufficient hardware resource slack margins and high-level software tool support must exist for the target DSP board architecture.

The high-level virtual prototypes of the system developed in MATLAB and Simulink allow the system designer to catch hardware/software integration errors early in the design process. This ap-

proach allows for low-level performance limitations to be identified and corrected before costly hardware packaging assembly and field testing.

Case Study: Synthetic Aperture Radar Processor

Synthetic Aperture Radar (SAR) is an important tool for the collection of high-resolution, all-weather image data and is applicable to tactical ISR

systems. In addition, SAR can identify man-made objects on the ground or in the air. Such object identification typically requires real-time processing by means of a high-performance, embedded signal processor. Most SAR image and product formation algorithm steps are independent and separable, making them good candidates for parallel computation on multi/many-core processing platforms.

This case study considers the design of an SAR processor that must form high-resolution images in real time on board an aircraft. The algorithm's three principal stages are video-to-baseband IQ conversion, range processing and azimuth compression processing. Each SAR data pulse consisting of 8,192 data real video samples is converted to complex samples at baseband. Range processing transforms each complex SAR data pulse into a compressed range pulse consisting of 4096 complex samples. Then, azimuth compression, using cross-range convolution filtering, places compressed range pulses in time sequence into a 2D (4096 x 2,048) processing array and convolves each row of the array with a row-specific reference kernel. The convolution outputs are saved in an image array, which becomes the output strip-map image of the SAR.

The SAR processing system then applies ISR specific processing to the output strip-map image including auto-focusing, polarimetric whitening filtering and target detection processing. Autofocus algorithms improve image focus by removing phase errors present after conventional motion compensation. Polarimetric whitening filters improve SAR radiation resolution by reducing image speckle after auto-focusing. Automatic target detection techniques then process the enhanced SAR images, identifying time-sensitive ISR targets in real-time.

ISR-Specific Processing

At its maximum Pulse Repetition Frequency (PRF) of 4,535 Hz, the radar delivers 1,024 pulses with 8,192 data samples for each of the four polarizations in 226 milliseconds. The processor must

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form a 1,024-pulse image for each of four polarizations in real time with a latency not greater than two seconds. Given a maximum PRF of 4,535 Hz for the radar, the real-time constraint on video-to-based IQ conversion and range-processing tasks is 221 microseconds, and the real-time constraint on the azimuth processing and ISR specific processing tasks is 226 milliseconds. The computational requirement of the algorithm is about 85 Gflop/s. The memory requirement is approximately 3.4 Gbytes.

Table 2 provides a SAR processor implementation comparison of many-core GPU, multi/many-core GPP and multicore DSP technologies. Each SAR processor platform implementation is compared with respect to hardware procurement cost and software development cost and time. The comparison is restricted to single board processor implementations that can satisfy the real-time algorithm computational requirements, while minimizing SWAP. To minimize SAR processor development and lifecycle costs, which have traditionally been prohibitively expensive for FPGA and ASIC implementations, software-only solutions are highlighted in this comparison.

The COCOMO II software cost model was used to compute the software development cost and time estimates. Table 1 provides software tool usage effort multiplier values for the selected processor architectures. Table 2 includes software size estimates and execution time effort multipliers for each processor. For simplicity, all other software cost drivers are rated as nominal. The SAR case study comparison illustrates the impact that software tool support, DSP software library support and hardware platform constraints have on software development cost and time for high-performance ISR applications.

Real-Time Intelligence Analysis

Traditional DSP implementations for ISR systems can no longer keep pace with today's rapidly evolving threats. IvySys Technologies' Real-Time Intelligence Analysis methodology fully leverages this rapid prototyping methodology

to help the DoD and Intelligence Community detect and thwart continuously evolving threats and maintain tactical situational awareness. We automate the architecture selection and partitioning by incorporating software cost and development time models into a design optimization framework. This optimization approach exploits hidden efficiencies such as the front-end design process, which is typically less than 10 percent of the total

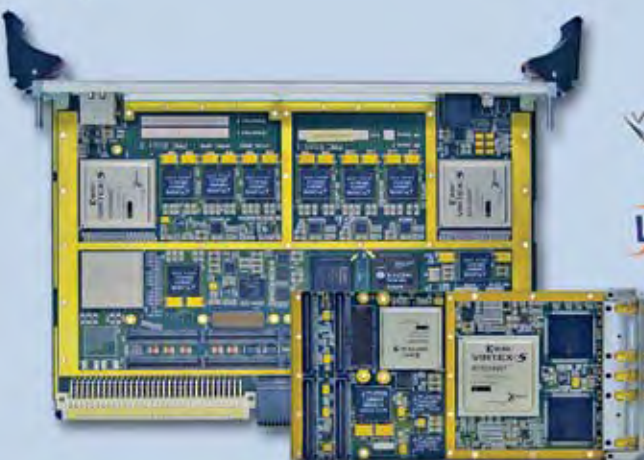
prototyping time and cost, but accounts for more than 80 percent of the system's lifecycle cost. In turn, it reduces development time and cost by as much as a factor of four. ■■


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System Development

Real-Time and Safety-Critical Challenges

Modular Approach Eases Avionics Certification Challenges

Reinventing the wheel every time is a costly and time-consuming approach to avionics design. The ability to do incremental certification is a key reason why an integrated modular avionics (IMA) system is so powerful and efficient.

Chip Downing, Director, Aerospace and Defense
Wind River

The promise of greater efficiency by using Integrated Modular Avionics (IMA) systems that reduce Space, Weight and Power (SWaP), is now coming to fruition. Very large, visible projects such as Boeing's 787 Dreamliner and Airbus' A380 are taking advantage of this more efficient strategy to integrate airframe suppliers' systems into shared airborne compute platforms.

The goal of IMA is to combine a number of traditional, stand-alone federated systems into integrated common platforms. This system reduction/compression increases power efficiency and reduces processor boards, support hardware and cabling, with the complementary benefit of reduced bill of materials (BOM) and number of Line Replaceable Units (LRUs), which simplifies spares management and training demands.

The most advanced IMA system to date, the Common Core System (CCS) supplied by GE Aviation for the Boeing 787 (Figure 1), is now running over 70 separate applications executing at separate safety levels. This architecture allowed Boeing to eliminate over 100 discrete LRUs on this state-of-the-art aircraft, and thus realize the savings in

SWaP as well as through-life costs associated with software updates, upgrades, maintenance, overhaul and repair.

The challenge of IMA is to maintain a servicing and replacement utility like federated systems have, while providing a robust mechanism for separation of applications of different safety criticality levels. Due to the extreme high costs of software testing and re-certification, a viable IMA platform must enable an efficient, cost-effective path to meeting RTCA DO-178B and DO-254 safety certification. This can only be done with incremental software certification.

Fundamental Changes

Under a federated avionics model, the subsystem hardware and software is delivered in a single package by a single prime contractor, who is responsible for 100% of the design, implementation and testing of the device; therefore, this federated systems supplier had full control over the development of the entire subsystem. This model tied the air frame manufacturer into a particular subsystem supplier and supply chain, which limited the options for cost savings, especially when it came to upgrading functionality or adopting new technology. New functionality was often solved by introducing a

new Line Replaceable Unit (LRU), which could be provided by the same manufacturer or put out to tender for procurement, both involving substantial costs.

In the federated supplier model (Figure 2), the LRU supplier for each system supported 100% of the responsibility for DO-178B and DO-254 certification of the unit. Typically, a single LRU would support one aircraft function, such as a Flight Management System; and although it could run several applications to support this function, it would be certified to a single DO-178B and/or DO-254 safety level. The LRU supplier would then take the entire system through the certification process and provide this evidence to the airframe manufacturer for inclusion in the aircraft safety case.

Incremental certification was not possible—every time a line of software code needed to change it forced, by DO-178B and/or DO-254 guidelines, a complete requalification of the entire LRU. This is true even if the LRU compute platform implemented an application partitioning strategy, usually due to control and/or data coupling between these applications and the operating environment. Any change in the board support package (BSP), real-time operating sys-

tem (RTOS)/scheduler, or in the application, forced a retest of the entire LRU software stack.

New Approach: IMA

With the newer approach of IMA, the applications are separated from the base computing platform, communicating through the standard ARINC 653 API, and controlled, using a time and space scheduler, by the ARINC 653 RTOS (Figure 3). This separation enables the airframe manufacturer to potentially procure the base computing platform and applications from separate sources, picking the best-in-class supplier for each function. This IMA architecture allows a greater range of competition and flexibility for the airframer, but does increase the challenges of software engineering and systems integration, including deploying airborne units where competitors share the same compute silicon.

Shared IMA compute platforms have necessitated a dramatic shift in the way aircraft systems are developed, with new, specific roles defined for the systems integrator, platform supplier and application suppliers; these roles are defined completely under the DO-297 standard titled, "Integrated Modular Avionics (IMA) Development Guidance and Certification Considerations." Under this model, adding more functionality to the system involves adding, or modifying, an existing software application. The challenge then becomes how that software component is designed, tested and integrated into the final system, without impacting the safety or security of other applications or for the platform itself.

Separating Responsibilities

Each of the roles has defined responsibilities for the certification of their component. The platform supplier handles the delivery and certification of the base platform (hardware and software), the application suppliers are just responsible for their application, and the systems integrator is responsible for consolidation of all the safety artifacts from these separate sources to provide an overall safety case to the customer.



Figure 1

The most advanced Integrated Modular Avionics (IMA) system to date is the Common Core System (CCS) supplied by GE Aviation for the Boeing 787. It runs over 70 separate applications executing at separate safety levels. This architecture allowed Boeing to eliminate over 100 discrete LRUs on this state-of-the-art aircraft.

As a result, the IMA approach of putting multiple separate safety-critical software applications on a single hardware platform has led to much stricter contracts between these separate components, at both the business and system levels. Although this stricter contract and separation between the components gives the systems integrator the challenge of allocating resources among all of the application suppliers, it does provide a platform that may allow each of these applications to be safely certified to a different level. IMA platforms also introduce the capability of incremental certification, where the retest of the entire platform is not required, only a test of the scope of any application change.

Incremental Certification

ARINC 653 architectural robustness per DO-178B guidelines is the key to incremental certification efficiency. Without this proven separation, ARINC 653 systems are automatically converted to very complex and unmaintainable

federated platforms, and every change to the integrated platform forces a retest of the entire platform, causing an exponential increase in system testing, rendering the integrated platform not commercially viable.

Robustness, as defined under DO-178B guidelines, is a very specific proof that under all application failure conditions, a single failure in one partition will not affect other partitions. This can be a challenging endeavor to prove, and in the case of Wind River's VxWorks 653 certification evidence, this document is over 330 pages in length, and includes testing and analysis for both the ARINC 653 RTOS provider (in this case, Wind River), and specific tests to be performed on the airframe deployment hardware.

Incremental certification only works if the hardware and software components are truly isolated, enabling the proven independence or robustness of the entire system. This separation means the software has to be developed without relying on specific hardware or other appli-

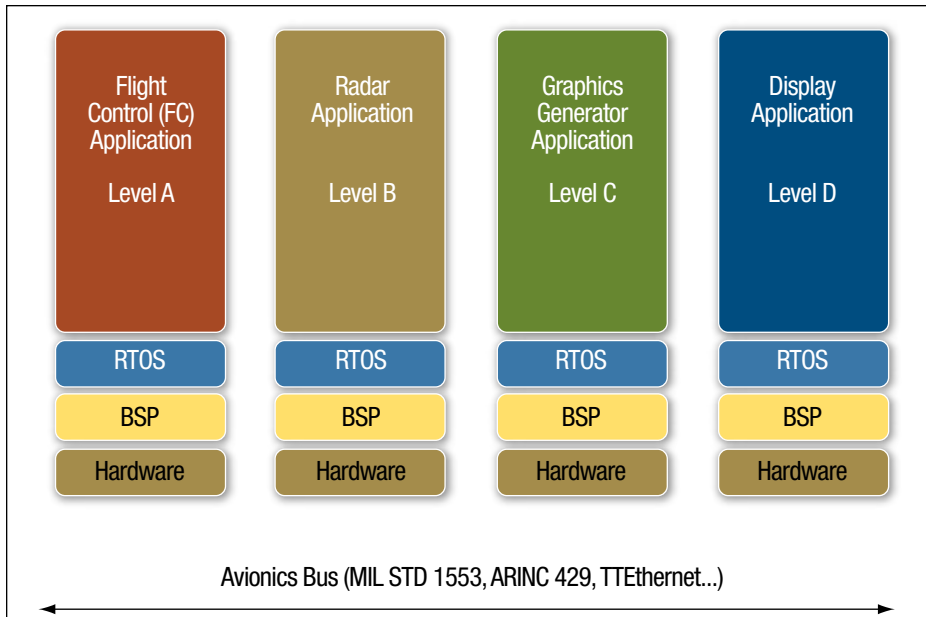


Figure 2

In the federated supplier model the LRU supplier for each system supports 100% of the responsibility for DO-178B and DO-254 certification of the unit. Although an LRU could run several applications, it is certified to a single DO-178B and/or DO-254 safety level.

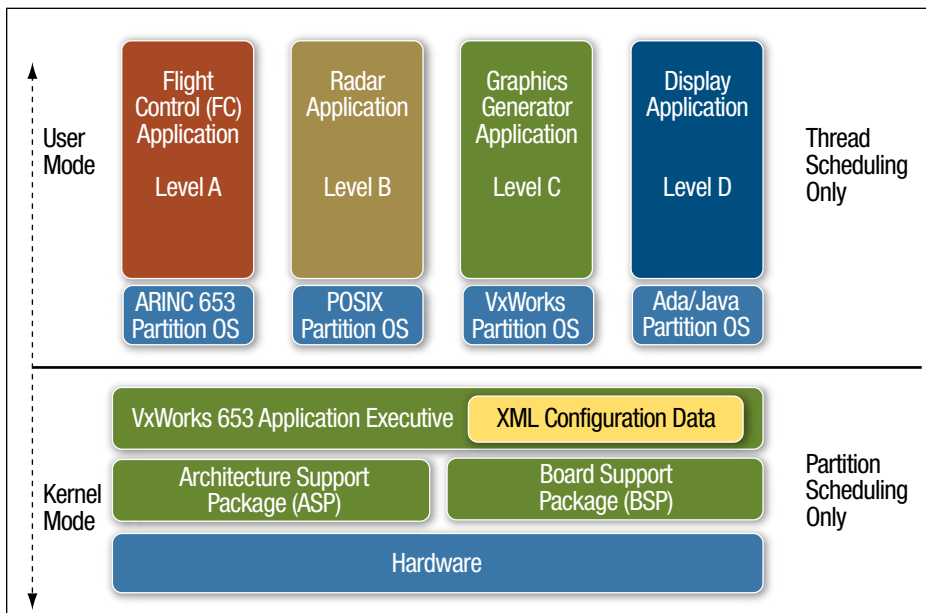


Figure 3

Using the newer approach of Integrated Modular Avionics (IMA), the applications are separated from the base computing platform, communicating through the standard ARINC 653 API, and controlled, using a time and space scheduler, by the ARINC 653 RTOS.

applications at build time, instead using only the computer resources provided by the base platform, through standard ARINC 653 Application Programming Interfaces

(APIs). These resources would include not only the ARINC 653 APIs themselves, but provide access to hardware resources such as CPU, memory and I/O.

The first challenge of robustness is to provide access to these resources, using the ARINC 653 APIs so that applications can get access to these resources and meet their designed performance requirements. This is challenging both from a perspective of defining a strategy for sharing resources across the platform without impacting the robust partitioning, but also achieving this without reducing the performance requirements of the applications.

The second challenge is how to build, configure and deploy the application in an IMA system so that applications can readily move from one platform to another, and applications can be modified without changing or affecting either the base platform, or other applications. This is where the platform supplier has the challenge of mapping these I/Os and other system computing resources to the ARINC 653 API, as well as providing other APIs for ease of migration of other software assets (such as POSIX or Vx-Works applications).

The systems integrator then has the challenge of integrating these applications onto the base platform, and making sure that the overall system still meets its performance requirements. This activity could involve a complex negotiation between these separate suppliers in order to allocate the resources efficiently. Decisions here can also impact the overall configuration of the shared computing platform and require the platform supplier to provide more CPU resources or to distribute the applications differently on the final system.

The Whole Lifecycle

Having a simple ARINC 653 application API on top of an RTOS, or having an ARINC 653 operating system that just provides time and space partitioning at the application level, is not enough. It must support an environment where not only system components are robustly separated, but also the software development lifecycle needs to be separated, fully enabling incremental certification. This is the fourth challenge and requires a more sophisticated design environment where applications can be devel-

oped and tested without relying on the existence of other applications or specific hardware.

Often there are implicit, unseen, or otherwise unknown links or coupling between applications, BSPs and drivers that nullify true application and system independence; robust partitioning requires that no control or data coupling be between partitions. Control coupling is defined as vulnerability to external access, such as overrunning allocated time slots, while data coupling includes shared data as well as stacks and processor registers. Any control or data coupling between the IMA platform components removes the possibility of DO-178B partitioning robustness, and therefore incremental certification.

From Boeing 777 to 787

Despite all the challenges, a prime example of the benefits of adopting an IMA approach is the evolution of the Boeing 777 to the 787. While the 777 had IMA for the flight management systems, the current IMA development for the 787 is running approximately 70 applications on a single avionics hardware platform, combining the navigation systems, electrical power distribution and waste management systems. This architecture has allowed Boeing to eliminate discrete LRUs and thus realize savings in SWaP and through-life costs associated with maintenance, overhaul and repair.

The longer term benefits of using an IMA approach for aircraft system design are now well-defined. Reducing SWaP by eliminating scores of separate processor units has a tremendous positive impact on the efficiency and profitability of the aircraft during its lifetime, as well as enhancing software systems' engineering capability among the global supply chain.

A New Way of System Design

This has required a fundamental shift in the way these systems are specified, designed, implemented and tested, which has required years to implement at its highest efficiency in order to maintain the high safety levels mandated in the avionics industry. Each product gen-

eration increases the level of integration, while supporting associated increases in complexity and in certification testing. The software in the current generation of aircraft is probably the most rigorously tested software on the planet.

These changes, not just in the technology, but also in the standards, business model and certification strategies, all advance at different speeds. However, these IMA advances have made significant in-

creases in efficiency when implemented with robust separation and incremental certification as proven by the latest-generation aircraft implementing these global IMA standards and practices. ■■

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System Development

Real-Time and Safety-Critical Challenges

Addressing the **Application Side** of the MILS Architecture

Although the MILS architecture has become well understood, developing applications for it can be a challenge. The language features of Ada and SPARK help smooth the way.

Greg Gicca
Director of Safety and Security Product Marketing
AdaCore

Several real-time operating systems (RTOSs) on the market today support the Multiple Independent Levels of Security (MILS) architecture. Many of these have been certified (or are plan to be certified) to support top security levels. These RTOSs provide the framework to support multiple applications running at different security levels on the same computer. However, little has been published on how to create and certify new applications on top of this architecture to top security levels.

In a general sense a MILS architecture supports running different applications on a single computer at different security levels. It further supports policy-based and controlled communication among these applications. The core architecture is often graphically portrayed as a thin kernel layer on top of a processor with walled-off blocks that represent partitions isolating different applications

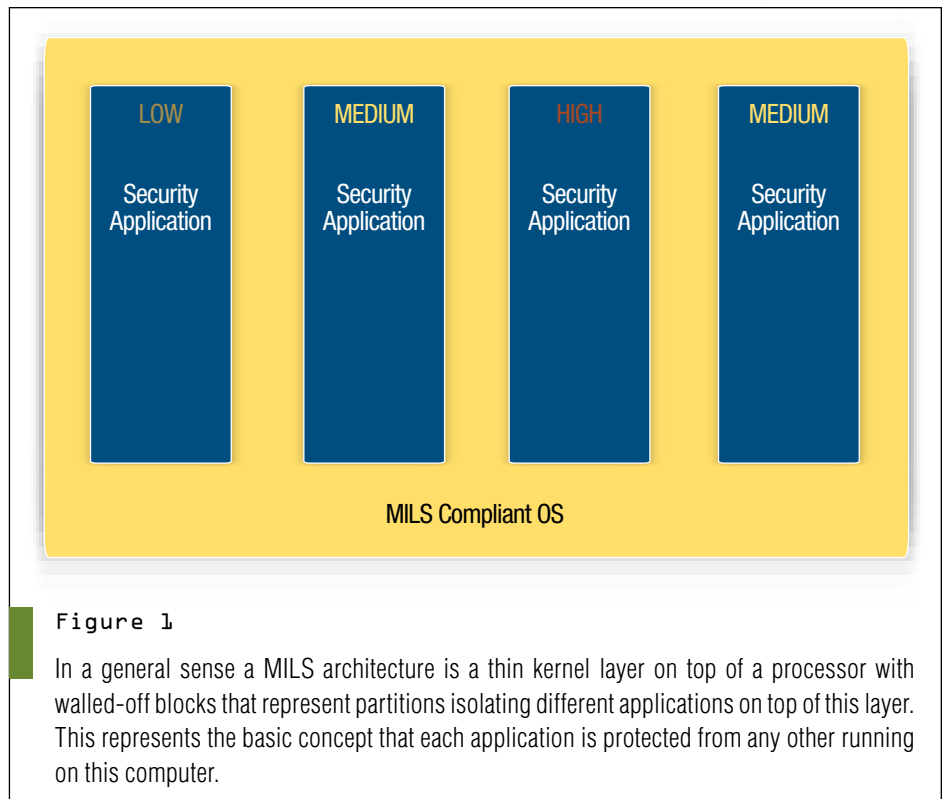


Figure 1

In a general sense a MILS architecture is a thin kernel layer on top of a processor with walled-off blocks that represent partitions isolating different applications on top of this layer. This represents the basic concept that each application is protected from any other running on this computer.

on top of this layer (Figure 1). This represents the basic concept that each application is protected from any other running on this computer.

Policy-based communication is supported by a capability separated

from the individual applications but available to them. Other typical shared resources are also made available in their own partitions. As an example, the inter-partition communication may support the policy of passing data from

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EAL	Requirements
1	Functionally tested
2	Structurally tested
3	Methodically tested and checked
4	Methodically designed, tested, and reviewed
5	Semiformally designed and tested
6	Semiformally verified design and tested
7	Formally verified design and tested

Figure 2

NIAP (a NIST/NSA partnership) has defined a set of Evaluation Assurance Levels (EAL) ranging from 1 to 7, or low to high.

a low security partition to a higher rated one while preventing high-security data from being passed to a lower-rated security partition. The available shared resources might provide access to storage devices, external communication

supplied by Ethernet, or other common system services.

The key technological concept behind the architecture is that each partition provides a specialized capability. Each may be implemented by a small

application with a simpler logic. In this way each provides a useful capability but is small enough to be certified to top security levels. When assembled, the total architecture provides a demonstrably secure platform for supporting the desired multiple applications running at different security levels. This divide-and-conquer approach to certification is a well established solution throughout various engineering disciplines.

A MILS architecture provides a foundation for supporting multiple applications at different security levels. The certification of each application to the required security level is not addressed in the architecture definition. Previously certified applications may be ported to operate within a MILS partition. New applications will need to be developed to meet specific security requirements as applicable to the security level. NIAP (NIST and NSA partnership to evaluate IT product conformance to international standards) has defined a set of Evaluation Assurance Levels (EAL) ranging from 1 to 7, or low to high. In brief, these are defined as shown in Figure 2.

Lower levels of EAL (1-3) only require testing and can be developed using a variety of development paradigms and tool sets. EAL 4 requires a thorough process and exhaustive testing. This level is basically equivalent to the requirements for the airborne avionics DO-178B safety standard Level A. Thus, applications developed to this standard may be supported in a MILS partition and certified to EAL 4. If an application needs to meet both safety (in particular DO-178B Level A) and security requirements, this might be a sound development and certification approach. Applications needing to meet EAL 5 or higher will need to be developed using stricter approaches. Software for the advanced Air Refueling Boom System (ARBS) (Figure 3) built by EADS CASA employed AdaCore GNAT Pro High-Integrity Edition for VxWorks653 in the development of its device software.

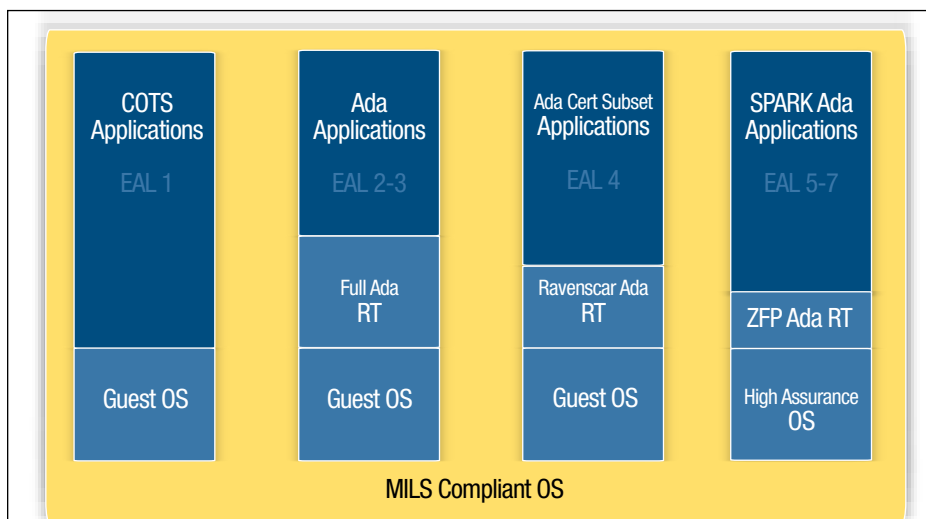


Figure 4

An example distribution of different security level applications within a MILS architecture.

This software is certified up to Level A of RTCA DO-178B.

Applications needing to meet EAL 5-7 require the use of semi-formal or formal methods as applicable to their certification level. Use of general-purpose programming languages and methods are possible but may be extremely costly to prove correct at these levels. Languages and tool sets that support semi-formal or formal methods can reduce the cost of high-security application development and certification.

SPARK is a formal-methods-based programming language and accompanying tool set designed to support the development of safety- or security-critical software. The SPARK language and tool set help prevent, detect and eliminate defects early in the lifecycle as the source code is developed. It is, effectively, the result of applying the principles of Correctness by Construction to the design of a programming language and associated verification tools.

Syntactically and semantically, the SPARK language is a subset of the Ada programming language, augmented by specially processed comments (“contracts”), and is fully deterministic and verifiable. Ada was chosen as the basis for SPARK because of its clear syntactic and semantic definition as an ISO language standard, and its many features that help program reliability. Features that complicate verification (for example, exceptions) are excluded from SPARK, but the language does include a simple set of Ada’s tasking features, known as the Ravenscar profile, that are amenable to certification. SPARK’s contracts include a set of pre- and post-condition annotations that may be used to more fully define an application’s logic and information flow. SPARK has a proven track record as a verifiable language suitable for top security application development and certification.

Above EAL 4 an application’s security functions must be shown to be correct with increasing amounts of rigor. What requirements must be met depends on the application itself and



Figure 3

Software for the advanced Air Refueling Boom System (ARBS) built by EADS CASA employed AdaCore’s GNAT Pro High-Integrity Edition for VxWorks653 in the development of its device software. This software is certified up to Level A of RTCA DO-178B.

the desired EAL. Different application areas have defined sets of associated test areas or qualifications that must be demonstrated. These collections of test areas are termed Protection Profiles. These provide a set of qualifications

that can be viewed informally as test areas that must be shown correct. Protection Profiles have been developed for various application types, such as operating systems, communication services and security utilities (firewalls, etc.).

Each Protection Profile has an associated application area and security level or EAL that conforming applications can meet.

New applications needing to meet an EAL of 5 or higher will greatly benefit from a programming language that supports proof of the application logic properties.

The SPARK language meets this goal. Applications at lower EALs can be written in any programming language and may in fact be existing programs ported to the MILS architecture from other platforms. These could be off-the-shelf applications such as word processors, spread sheets, or entertainment programs.

At higher EALs these applications could again be existing programs but now more thoroughly tested to meet specific security testing requirements. EAL 4 applications are high-reliability programs that must be shown to meet exacting safety or security requirements. These again might be applications from another platform ported to the MILS architecture but developed using a strict process and thoroughly tested. Programs needing to satisfy EAL 5 or higher should be developed with security in mind from the onset.

Although any programming language can be used for lower EAL, the Ada programming language is a good match across the full range of EALs. Lower levels may use the full power of Ada, including concurrency features (tasking), full object oriented programming, generic templates, exceptions, etc. As the EAL increases stricter subsets can be used. At EAL 4, full tasking and generics might no longer be appropriate. Their elimination allows for less costly testing and verification. At EAL 5 this same subset may be appropriate, but some form of proof of correctness must be introduced. SPARK provides exactly this functionality.

The Ada language generally is accompanied by a runtime library, a small executive to support various language features. As the EAL increases, features that require this layer should be eliminated to simplify testing or proof of correctness. Applications above EAL 5 should use no feature that requires runtime support. SPARK meets this criterion and can thus be used for application development and certification at EAL 5 through 7. Figure 4 shows an example distribution of different security level applications within a MILS architecture.

In summary, the use of the SPARK language provides a unique capability to develop applications to top EAL on top of a MILS architecture. At lower EAL any application language may be used to satisfy the much less stringent qualification requirements for these levels. Existing

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applications from other platforms may be the ideal solution for these levels. At mid-range levels the thorough development process and testing requirements imply that applications use a language and be developed with safety or security in mind at the onset. As such they tend to be developed specifically for this purpose and the associated certification requirements for the area.

At EAL 5 and higher the language used for application development should support the proof of correctness demanded. This is not required but will reduce the overall cost of either development or certification in the end. It is interesting to note that a single programming language base can be used across all EAL. The full Ada language offers powerful features to develop sophisticated applications at low EAL. As with any language some of this power and features make testing or proof of correctness more difficult at higher levels. Thus full Ada is not appropriate for mid-range EAL. A subset can be defined and used at these levels. Top EAL are more easily developed and certified using a language that supports proof of properties of the application logic. The Ada language cannot support this directly. The SPARK language is defined explicitly to support this rigor. Where SPARK uses the Ada language as its core definition, a single language may be used to develop applications at all EAL for a MILS architecture.

The MILS architecture and application development support for all EAL is an ideal solution for a wide range of military applications. Immediately it helps solve the issue of combining multiple computer systems in a secure way. These may be existing or COTS applications for lower security levels or custom security certified applications for higher levels. Military avionics applications can take advantage of combining applications to separate secure communications from other more general systems as well as implement flight-critical applications within an EAL 4 or higher partition. MILS has wide applicability

across many domains where combining computer systems and applications can save on total systems cost. The use of the Ada language and specialized languages such as SPARK, allows for the creation of multiple levels of secure applications using a single programming language base. ■■

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Technology Focus

OpenVPX Boards

OpenVPX: Cards Dealt, Ready to Play

With the OpenVPX Spec now ANSI-ratified and new products galore, OpenVPX is positioned to become the next dominant computer form factor for new military system designs.

Jeff Child,
Editor-in-Chief

Hailed as the next-generation fabric-based slot card standard, VPX has had a few rocky years getting started. But over the last year and a half, the goal of bringing together advanced switch fabric interconnects and all the features of a modern, rugged embedded computer architecture, finally came together in the form of OpenVPX. Over that time, a group of military embedded computer vendors and prime contractors, first under the OpenVPX Industry Working Group, morphed the VPX 46 architecture into an interoperable system-level specification called OpenVPX.

Last month OpenVPX achieved its final milestone with the ratification by ANSI of the OpenVPX System Specification under ANSI/VITA 65.0-2010. OpenVPX provides implementation details for VPX payload and switch modules, backplane topologies and chassis products. And most importantly, it provides specific profiles on all the key aspects of an OpenVPX so that users and product vendors now have a clear language defining which OpenVPX are compatible with one another (Figure 1). In doing so, OpenVPX solves the long-known problem that has faced VPX from its inception: With its large number of open pins and the variety of fabric options available to it, it's difficult to ensure any compatibility between VPX products of different vendors. The spec provides defense primes and suppliers clear direction for crafting interoperable computing and comms platforms.

In support of the VPX family of specifications, VITA members have been rolling out a wide range of products suited to a variety of applications, from backplanes and chassis to 3U and 6U boards of various types. Nearly 100 products are already available and more are added each week. With the completion of this specification, suppliers are now identifying their products with the profile information necessary to make product selection for specific profiles.

The VPX standard was developed to define a new generation of computing systems that employs high-performance switch fabrics over a new high-speed connector, as well as operates in harsh environments. Which OpenVPX fabric to use will be dictated by the application area of the system. And on an architecture level, the fabric choice will be driven by how tightly or loosely coupled the



Figure 1

For UAV control systems, PCI Express will be the likely OpenVPX fabric of choice. Shown here, an MQ-9 Reaper UAV sports a set of GPS-guided GBU-49 weapons.

processing and memory needs to be. For applications that require shared memory, RapidIO will be the data plane of choice. In contrast, if the system requires parallel processing—where very little data exchange is required between computing nodes—a fabric like PCI Express, Gbit Ethernet or 10 Gbit Ethernet is a better choice.

For OpenVPX implementations that are distributed systems, PCI Express would be a natural fit depending on what size and what latency tolerances a system has. With PCI Express, each time you go through a switch or a bridge means more latency through the PCI hierarchy. That latency can be minimized using non-transparent PCI Express bridges or by “tunneling” through address spaces. Distributed processing is common in systems where size, weight and power are critical—like UAVs (Figure 1), flight controllers and other systems that have motors and distributed control nodes. In such systems computational density is important, but not to the level of high-performance computing. ■■

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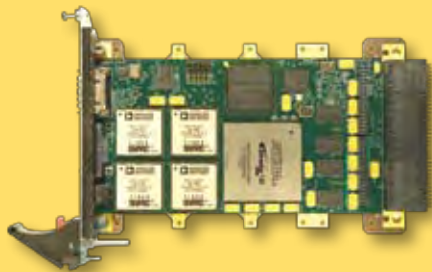
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Technology Focus:

OpenVPX Boards Roundup

FPGA and TigerSHARC Share 3U VPX Board

FPGAs and DSPs have different strengths when it comes to the signal processing muscle they provide. BittWare has brought together the best of those worlds with a hybrid system sporting both a high-end FPGA and the TigerSHARC DSP with the release of the GT-3U-VPX (GT3X) board. The GT3X features a large Altera Stratix II GX FPGA and one cluster



of four ADSP-TS201S TigerSHARC processors from Analog Devices. The front panel provides high-speed SerDes, 10/100 Ethernet and RS-232; and the extensive back panel interface supports PCI Express, Serial RapidIO, GigE and 10 GigE. The GT3X can achieve simultaneous on-board and off-board data transfers at rates exceeding 2 Gbytes/s via BittWare's ATLANTiS FrameWork implemented in the Stratix II GX FPGA.

The GT3X provides a hybrid signal processing architecture that takes advantage of both FPGA and DSP technology, creating a complete solution for applications requiring flexibility and adaptability along with high-end signal processing, all on a ruggedizable platform.

BittWare
Concord, NH.
(603) 226-0404.
[www.bittware.com].

OpenVPX 3U VPX-REDI Board Sports AtomZ530

A lot of momentum has gathered around the newly completed OpenVPX specification. Concurrent Technologies has introduced a low-power 3U VPX-REDI SBC, the TR A40/30x RC, designed to comply with the OpenVPX VITA 65 standard. The TR A40/30x RC utilizes the 1.6 GHz Intel Atom processor Z530 and the highly integrated Intel System Controller Hub US15W both from the Intel embedded roadmap, ensuring long-term availability. The board supports up to 2 Gbytes DDR2-533 soldered SDRAM and a wide variety of I/O interfaces, including a CANbus interface, yet maintains a typical power requirement of less than 10W.



The RC-Series TR A40/30x RC is a VPX REDI Type 1 Two Level Maintenance conduction-cooled board with support for Built In Test (BIT). The TR A40/30x RC SBC provides a flexible PCI Express OpenVPX backplane fabric interface that can be configured for several OpenVPX slot profiles from 8 x1 PCIe ports through to 2 x4 PCIe ports. The VITA 46.0-compliant TR A40/30x is an air-cooled SBC designed for non-rugged environments operating over a temperature range of 0 to 55°C. The pin-compatible TR A40/30x RC is designed as a conduction-cooled SBC for rugged environments and operates over temperatures of -40° to +85°C and at altitudes from -1,000 to 50,000 feet.

Concurrent Technologies
Woburn, MA.
(781) 933 5900.
[www.gocct.com].

Serial RapidIO GEN-2 Switch Rides OpenVPX/VITA 65

With OpenVPX well on its way to final ANSI approval, a flurry of OpenVPX products is feeding the OpenVPX ecosystem. Curtiss-Wright Controls Embedded Computing has announced the availability of the new OpenVPX/VITA 65-compliant VPX6-6902 Serial RapidIO (SRIO) switch card. This rugged 6U VPX board, available in both air- and conduction-cooled versions, combines



Ethernet and SRIO switching in a single slot for management, control and dataplane switching in high-performance embedded military systems. Supporting both Gen-1 SRIO (1.25, 2.5, 3.125 Gbaud) and Gen-2 SRIO (5.0, 6.25 Gbaud), the VPX6-6902 enables systems integrators to quickly and easily architect small to large high-performance systems that adhere to the VITA 65 OpenVPX systems specification.

SRIO is a next-generation data-plane interconnect and combines extremely high data rates with low system latency. Eclipsing existing Generation 1 SRIO switches, the VPX6-6902 doubles the available bandwidth with SRIO Gen-2 technology, offering up to 20 Gbit/s throughput on each of its 28 4-lane ports. The VPX6-6902 is designed to form the interconnect backbone of extremely high-performance mission computing environments, and simplifies systems design with features designed for redundant and fail-safe architectures.

Curtiss-Wright Controls
Embedded Computing
Leesburg, VA.
(703) 779-7800.
[www.cwembedded.com].

OpenVPX Module Sports 8-Core P4080 Processor

Multicore processors are the new norm in CPU technology, and military system developers are embracing the trend wholeheartedly. Extreme Engineering Solutions has announced the XPedite5470, a high-performance 3U OpenVPX single board computer with Freescale QorIQ P4080 processor. XPedite5470 provides a new level of Power Architecture computing power with features including a Freescale P4080 processor with eight Power Architecture e500 cores at up to 1.5 GHz.

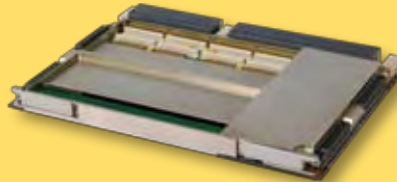


Memory on board includes 8 Gbyte DDR3-1333 ECC SDRAM in two channels and 256 Mbytes of NOR and 16 Gbytes of NAND flash. Hardware write-protection is provided for NVRAM. The card provides Serial RapidIO, x4 PCI Express and SerDes Gigabit Ethernet interconnects as well as Ethernet and serial ports. All of X-ES's P4080 products are engineered to scale from air-cooled commercial (0° to 55°C) to full conduction-cooled (-40° to +85°C) with appropriate shock and vibration testing.

Extreme Engineering Solutions
Middleton, WI.
(608) 833-1155.
[www.xes-inc.com].

OpenVPX SBC Sports 2.53 GHz Core i7 Processor

The Intel Core i7 processor invaded the military embedded computer arena faster than any of its predecessors—a sign that performance at low power is in high demand. GE Intelligent Platforms offers the SBC622, a rugged 6U OpenVPX-compliant single board computer. Based on the powerful Intel Core



i7 processor, it is designed to play a key role in the rapidly developing field of network-centric warfare in which data-driven architectures enable warfighters to gain a more complete realization of the battlefield environment. Typically challenging applications include early warning systems, command and control, and the aggregation, analysis and dissemination of real-time sensor data including radar, sonar and video in air, sea and ground applications. Such applications demand outstanding processing capability, comprehensive I/O and communications and absolute reliability.

At 2.53 GHz, the SBC622's Intel Core i7 processor is 30 percent faster than its predecessor, while double the memory capacity—up to 8 Gbytes of soldered DDR3 SDRAM with ECC—of first generation VPX single board computers further enhances performance. Optimum scalability and interoperability are delivered by the SBC622's high-bandwidth 10 Gigabit Ethernet I/O fabric subsystem. Customer flexibility to configure the SBC622 according to the precise requirements of the application is delivered via two onboard PCI-X PMC/XMC mezzanine expansion sites. Compliance with the OpenVPX standard ensures that the SBC622 is interoperable with a broad ecosystem of solutions. Available in five rugged air- and conduction-cooled build levels for optimum cost-effectiveness, the SBC622 is fully supported by comprehensive Deployed Test Software (BIT and BCS).

GE Intelligent Platforms
Charlottesville, VA.
(800) 368-2738.
[www.ge-ip.com].

VPX-REDI SBC Enables Network Connectivity Mobile Apps

The ecosystem for VPX continues to grow and more and more vendors roll out their VPX offerings. Designed to withstand the rigors of mobile and tactical environments, General Dynamics Canada introduces the new rugged and powerful PX3030 VPX-REDI single board computer. The PX3030 harnesses the computing power of the Intel Core 2 Duo Mobile processor and 8 Gbyte RAM to easily handle today's demanding network communications, graphics, imagery and video feeds needed for Modern Brigade Combat teams.



The board is aimed at applications such as tactical wheeled vehicles including tanks, expeditionary fighting vehicles and Stryker platforms as well as armament platforms such as mobile gun systems and cannons. Other applications include airborne command and control for combat helicopters, aircraft and unmanned aerial vehicles. Features of the board include dual Gbit Ethernet 10/100/1000 connectivity, onboard storage up to 16 Gbytes of SATA NAND flash, six USB 2.0 and four RS-232/422 ports. The card meets VITA 47 CC4 vibration, shock and temperature specs. It's a 3U module per VITA 48.2 (conduction-cooled), Type 1, 0.85-inch pitch. Compatible software includes Microsoft Windows, LynuxOS, Linux, HHEL, VxWorks and other operating systems.

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1 GHz PowerPC MPC8536E Rides 3U VPX

The PowerPC platform enjoys a rich legacy among military programs. Interface Concept has introduced the IC-PQ3-VPX3a, an ultra-low-power Processor VPX 3U board based on the Freescale PowerQUICC III MPC8536E processor. The IC-PQ3-VPX3a is designed to offer both the gigahertz-class complex application processing abilities and high-speed connectivity in a small board footprint. Typical consumption in full-operational configuration (1 GHz) is 10W.

The IC-PQ3-VPX3a is ideally suited for a large range of embedded applications such as compute-intensive solutions requiring high-speed I/O transactions, Gigabit Ethernet interfaces for high-performance network connectivity or redundant failsafe links,



powerful control element for network switches, storage subsystems, network appliances, print and imaging devices, etc.

Other features include up to 1 Gbyte DDR2-ECC, 128 Mbyte flash, 4 Gbytes of NAND flash and up to three Gigabit Ethernet ports. The IC-PQ3-VPX3a is available in standard, extended and rugged grades. Interface Concept provides BSP for VxWorks and Linux operating systems. Other RTOS can be ported on request.

Interface Concept
Briec de l'Odet, France.
+33 (0)2 98 57 30 30.
[www.interfaceconcept.com].

OpenVPX IPv4/v6 Switch Offers 28 Gigabit Ethernet Ports

The military has embraced Ethernet in a big way, not just as a networking technology, but as a high-speed interconnect fabric as well. The new Kontron Gigabit Ethernet Switch VX3910 offers 3U VPX (VITA 46.x) and OpenVPX (VITA 65) platforms Enterprise-Class Switching functionality with a total of 28 Gigabit Ethernet ports and advanced management features. With its implemented Kontron Embedded Network Technology, which offers the same advanced feature set and operational interfaces across multiple form factors, it simplifies IPv4/v6 inter- and intra-platform networking.

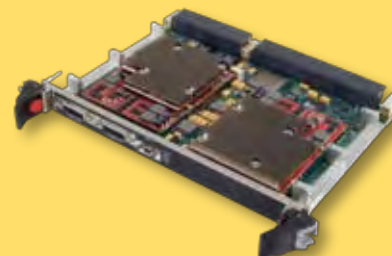


The non-blocking fully managed L2/L3 Gigabit Switch Kontron VX3910, with its 20x Gigabit ports to the backplane, offers the highest port density for the implementation of various network topologies in 3U appliances. Four additional 2.5 Gigabit ports to the backplane simplify a redundant system architecture with multiple switches with no single point of failure. The four 1000 Base-T uplinks on the front panel, one dedicated for out-of-band management, expand the range to a total of 28 ports. The new Kontron Gigabit Ethernet Switch VX3910 is available in an air-cooled version for ambient temperatures from 0 to +55°C and in a rugged conduction-cooled version for the extended temperature range from -40° to +85°C.

Kontron America
Poway, CA.
(858) 677-0877.
[www.kontron.com].

6U OpenVPX Board Provides GPU-Based Rugged Solution

OpenVPX has seen probably the fastest rate of new product roll outs in the last 12 months. The latest from Mercury is a high-performance 6U OpenVPX, dual GPU-based conduction-cooled subsystem. This subsystem is currently deployed in an embedded rugged defense surveillance platform, performing processing, exploitation and dissemination (PED). Mercury's scalable ISR subsystem is powered by the Ensemble 6000 Series GSC6200—an OpenVPX module powered by GPU technology



working in conjunction with Intel-based processing in a conduction-cooled, 6U form factor.

The subsystem currently delivers performance in the TeraFLOPS range, and the incorporation of GPUs enables the solution to be delivered in an optimized size, weight and power (SWaP) footprint. Mercury's innovative packaging technology on the GSC6200 leverages the easy-to-upgrade MxM GPU form factor, which enables customers to rapidly upgrade and deploy the latest and fastest GPUs from ATI or NVIDIA, resulting in even higher performance.

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Multifunction Boards Get ARINC429 Support

Semiconductor integration has enabled board-level products to cram multiple functions onto a single card. Along just such lines, North Atlantic Industries (NAI) has announced the availability of ARINC429/575 support for its wide range of OpenVPX, VME, cPCI and PCI Multifunction boards. Known as the A4, it joins an extensive list of functions that are currently available from NAI. The ARINC429/575 A4 provides up to six programmable ARINC429/575 channels. Each channel is software selectable for Transmit and/or Receive, High or Low Speed and Odd or No Parity, supporting multiple ARINC429 and 575 channels simultaneously.



One major advantage of this multifunction approach is higher functional density, which reduces overall board count, thereby saving space and cost, reducing heat dissipation and increasing overall system reliability. Other available functions include A/D, D/A, Synchro/Resolver/ LVDT/RVDT Simulation and Measurement, CANBus, MIL-STD-1553, Synch/Asynch RS232/422/485, Discrete, TTL/CMOS, Reference Generator, Differential Transceiver and Resistance Temperature Detectors (RTD). The ARINC429/575 function is supported on VPX, VME, cPCI and PCI Multifunction boards with operating temperature ranges of -40° to +85°C and 0° to +70°C. Pricing for 100 pieces of the 64C2 VME Board with 6 channels of ARINC429/575 support starts at \$2,880.

North Atlantic Industries
Bohemia, NY.
(631) 567-1100.
[www.naii.com].

VPX Software Radio Board Family Boasts Multi-Gbit Performance

Blending the requirements of rugged design and fast throughput, military software radio represents exactly the kind of application for which OpenVPX is suited. Feeding such needs, Pentek has introduced 14 products in their new family of 3U VPX boards for data acquisition, software radio and digital signal processing. These new boards offer flexible backplane fabric connections supporting maximum data rates of up to 4 Gbytes/s with PCI Express (PCIe) Generation 2 (Gen 2) and 2.5 Gbytes/s with other protocols.

Each of the new 3U x8 VPX modules features a PCIe Gen 2 interface. The PCIe interface includes a bridge that provides PCIe lane-width negotiation for x1, x4, x8 or x16 data transfers over the VPX backplane. All of the first 14



products announced offer a distinctive feature set with a wide range of capabilities: high-speed A/D converters from 105 to 500 MHz with 12- to 16-bit resolution; Xilinx Virtex FPGA products; D/A converters to 800 MHz with 16-bit resolution; wideband and narrowband digital downconverters and upconverters with channel counts from 2 to 256; and multi-frequency clock synthesizers from 20 to 500 MHz. These VPX products comply with the VPX REDI specification and can be supplied in both air-cooled and conduction-cooled versions. The starting price for the Model 5308 VPX to PC Adapter is \$5,490.

Pentek
Upper Saddle River, NJ.
(201) 818-5900.
[www.pentek.com].


UltraSPARC T2-Based VPX SBC Targets Mil Apps

This is truly becoming the year of VPX as vendors roll out many types of VPX products for military applications. Themis Computer has announced its new T2VPX 6U VPX board computer. The T2VPX is the first member of the company's new family of VITA 46-compliant, board-level computers. Themis' T2VPX supports the VITA 46 and VITA 65 standards, providing customers with next-generation processing performance and high-bandwidth serial switched fabrics. The board features a new system architecture that combines up to eight processor cores and 64 threads, with a VPX IO fabric. The T2VPX is ideal for compute-intensive military and aerospace applications requiring rugged computing solutions, beyond the reach of today's VME 64-based systems.

The T2VPX is based on the Sun UltraSPARC T2 CMT (chip multi-threading) processor, the industry's first "system on a chip" and runs both Linux and the Solaris 10 Operating System. Themis' new T2VPX board further proliferates Sun's advanced UltraSPARC T2 processor technologies into embedded computing markets. The T2VPX will be offered with 6 and 8 core processor options. T2VPX features and specifications include up to 32 Gbytes of DDR2 memory with ECC protection, onboard 1.8-inch HDD/SSD support, multiple Gbit and 10 Gbit Ethernet channels and more.



Themis Computer
Fremont, CA.
(510) 252-0870.
[www.themis.com].

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DDS Software Speeds Development of Real-Time Systems-of-Systems

Driven by initiatives like the Department of Defense's Global Information Grid, more and more systems are being integrated that were not originally designed to interoperate. Advanced middleware technology has made all the difference in a host of complex military System-of-Systems programs. Real-Time Innovations (RTI) has released version 4.5 of RTI Data Distribution Service. Version 4.5 introduces new features that significantly reduce the time and cost required to build and integrate real-time systems-of-systems. These features include new mediation capabilities to bridge between applications that natively support different external interfaces and protocols.

RTI Data Distribution Service 4.5 extends the capabilities of the market-leading implementation of the Object Management Group (OMG) Data-Distribution Service for Real-Time Systems (DDS) standard. RTI's DDS platform provides the integration infrastructure for more than 400 unique high-performance and mission-critical applications in industries that include defense and aerospace. With RTI Data Distribution Service 4.5, it is now easier to integrate these applications with each other and with applications that use non-DDS middleware, including legacy systems.

Real-Time Innovations, Sunnyvale, CA. (408) 990-7400. [www.rti.com].



USB Module Boasts Six Synchronous A/D Channels

Military data acquisition that used to require racks and backplanes can now be done on the desktop. Data Translation announces the DT9836S, the newest member of their popular DT9836 series of high-speed, high-performance simultaneous USB data acquisition modules. The DT9836S is a completely isolated high-speed USB module providing simultaneous analog inputs at up to 800 kHz per channel or 4.8 MHz total. Each analog input channel has its own separate A/D converter eliminating phase shift between each channel—a problem with multiplexed architectures where all inputs share one common A/D converter. As a result the DT9836 series can correlate measurements instantly.

Superior design quality for all error sources with an ENOB (Effective Number of Bits) rating of 14.4 bits and an SFDR (Spurious

Free Dynamic Range) of 95 dB are integral features of the DT9836S. The unit offers 800 kHz sampling per input channel and six true 16-bit analog inputs for measuring multiple channels simultaneously. 32 digital I/O ports are available for time stamping, pattern recognition and synchronizing external events. 500V galvanic isolation protects PC and maintains signal integrity. The DT9836S is available in two packaging configurations: a BNC connection and an OEM version, with pricing starting at \$2,025.

Data Translation, Marlboro, MA. (508) 481-3700.
[\[www.datatranslation.com\]](http://www.datatranslation.com).

Low Power, High Processing Combine on COM Module

Small form factor rugged boards continue to grow in importance in the military realm. A new ESMini module uses a PowerPC MPC5121e or a MPC5123 processor, each based on an e300 processor core incorporating a memory management unit (MMU) and a floating point unit (FPU) as well as a powerful 760 Mips using clock frequencies of up to 400 MHz. The MM50's soldered 512 Mbytes of DDR2 SDRAM withstands severe shock of 15g, 11 ms, bump of 10g, 16 ms and vibration of 1g from 10 Hz to 150 Hz (sinusoidal). ESMini modules, which measure only 95 mm x 55 mm, are firmly screwed to a carrier board and come with rugged, industry-proven and railway-compliant connectors with differential signals. Pricing for the MM50 is \$384.

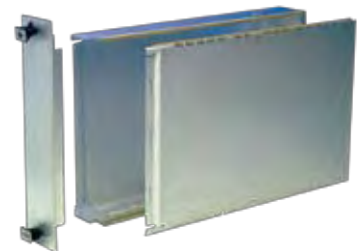
MEN Micro, Ambler, PA. (215) 542-9575. [www.menmicro.com].

VXI Module Shield Kits Comply to VXI-1 4.0 Spec

VXI remains a favorite technology for VME-based military instrumentation systems. ICS Electronics offers a new series of C-size VXI Module Shield Kits designed to comply with the recently approved Revision 4.0 of the VXI-1 Specification. These VXI4 Module Shield Kits are designed for the older 96-pin connectors as well as for the new 160-pin connector approved for VXI modules using the new 64-bit data bus. Typical uses are enclosing VXIbus modules to shield them from EMI/RFI emissions, to prevent a module from radiating RFI noise onto other modules or equipment and to provide mechanical structure to the module.

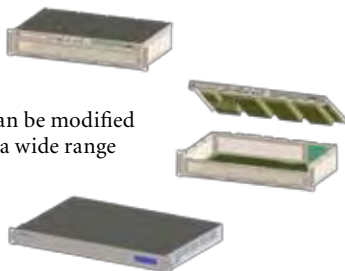
ICS's new VXI4 Module Shield Kits are a clam shell type design that surrounds the printed circuit board with RFI proof shields. Each kit includes the circuit side and component side shields, a blank front panel with ejectors, and all necessary hardware to assemble a VXI module. The connector shrouds have been removed to accommodate the wider 160-pin connectors. Generous air slots on the module sides provide for cooling air while limiting RFI emissions to 2 GHz. Pricing for the Single Slot Kit is \$250, the Dual Slot Kit is \$335 and the Triple Slot Kit is \$580. Prices listed are for quantities of 1 to 4 units.

ICS Electronics, Pleasanton, CA. (925) 416-1000. [www.icselect.com].



Enclosure Family for Desktop and Portable Cases

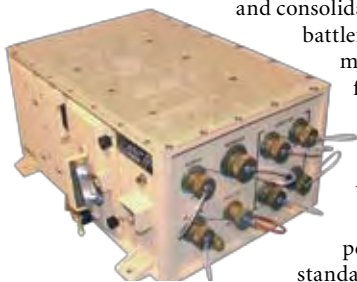
Elma Electronic offers a new customizable sheet metal enclosure platform. The Type 39 comes in desktop, portable and rackmount design options. It is an excellent enclosure platform for which to base custom designs. This family of chassis features advanced EMC options and ease-of-manufacturing, in a highly attractive, cost-effective package. The construction of the Type 39 was designed with EMC compliance as a primary consideration and can meet the strict requirements of CE and FCC. The standard front is powder-coated dark gray but can be modified to a wide range of color options. The enclosure family also has a wide range of handle styles and options. Various types of enclosure feet are available, including rubber, plastic, tilt and standard versions. Pricing for the Type 39 enclosure is under \$100 in volume.



Elma Electronic, Fremont, CA. (510) 490-7388.
[www.elmaelectronic.com].

Rugged Box Systems Target Mil Vehicle Apps

In recent years, the evolution of advanced applications has led to a proliferation of subsystems performing a variety of mission-critical functions in today's military vehicles. AP Labs has announced availability of the newest version of its Vehicle Expansion Unit (VEU) embedded computer system, which provides a rugged multifunction platform for deploying and consolidating applications within military vehicles used in harsh battlefield environments. The VEU supports efficient integration of multiple applications in a single rugged chassis, with scalability for up to three independent processors plus video encoding of up to four MPEG channels. Combining independent subsystems within a single thermally efficient fanless chassis provides a compact footprint for optimal Size, Weight and Power (SWaP) and improved maintainability. By offering a high degree of flexibility in processing power, data throughput, removable solid-state storage and standards-based interface options, the VEU supports a full range of vehicle-based applications, such as C4I, mission planning, data recording, vehicle maintenance & monitoring and real-time tactical display video streaming. At the AUSA in February, the VEU was demonstrated running Northrop Grumman's NCOMS-P software, providing fact-driven Condition-Based Maintenance (CBM) capabilities for operators/maintainers of military vehicles. The VEU also is used in a battlefield vehicle application that processes multiple video streams from externally mounted camera systems, thereby providing 360 degree observation in real time, even while traveling over rough terrain.



AP Labs, San Diego, CA. (858) 674-2850. [www.aplabs.com].

Atom-based Rugged SBC Is iPhone-Sized

For many of today's military applications, it's all about compute density. Feeding that need, General Micro Systems (GMS) has developed an Intel Atom-based rugged SBC that offers unbelievably low power consumption. Combined with its exceptionally small footprint and high performance, the Atom XPC40x (extended temperature, conduction-cooled) and Atom XP40x (standard temperature) satisfy the intense demand for an ultra-small computer with full-size processing power.

Easily accommodating 64 Gbytes of storage via onboard solid-state disk in its miniature 3.5 x 2.5 x 0.5-inch package, Atom is the world's smallest full-featured rugged computer. It boasts 533 MHz DDR-2 SDRAM and is powered by a 1.6 GHz Intel Atom processor that provides 512 Kbytes of Cache. With full laptop functionality, Atom offers high-performance graphics with 3D acceleration, and includes five USB-2.0 ports and support for two Express Mini Cards for Wi-Fi, CanBus or other user I/O. The Atom XPC40x is designed to operate at -40° to +85°C with a maximum thermal gain of only 5°C above ambient. Because of its heat tolerance, it is ideal for applications where ambient temperature is high, such as a controller located in an engine compartment or for small robots and UAVs working in extreme temperatures. The Atom, with its exceptionally low power consumption/dissipation (3W average, 10W peak), imposes little to no impact on the user, eliminating many inherent problems with wearable computers. Pricing starts at \$1,295 for the conduction-cooled XPC40x and \$695 for the standard-temperature XP40X in single quantities.

General Micro Systems, Rancho Cucamonga, CA. (909) 980-4863. [www.gms4sbc.com].



DIN Rail Power Supply Provides 30W and 100-277 VAC Input

TDK-Lambda has introduced a new low-profile DIN railmount power supply that operates off a wide range of AC input voltages, ranging from a nominal 100 to 277 VAC. The model DSP30-24/277A is rated at 30 watts and provides a 24 VDC output at up to 1.25A and is adjustable from 24V to 28 VDC. It is only 2.2 inches deep, making it ideal for installations in shallow enclosures commonly used in building, automation and security applications. The power supplies feature a universal input, allowing them to operate from any AC input voltage between 90 to 304 VAC, 47 to 63 Hz, without the need to reposition an input voltage selector. Because the units are Class II Double-Insulated, no earth ground wire is required. Operating efficiency for this supply is typically 87%. This supply is approved to UL60950-1, EN60950-1 and Evaluated to NEC NFPA70 Class 2 Output per UL1310.

TDK-Lambda Americas, San Diego, CA.
(619) 628-2859. [www.us.tdk-lambda.com].



4U Industrial Server Validated for High-Performance Computing

The Trenton TCS4500 industrial server is now available for deployment in computing applications requiring fast delivery as well as performance and long-term system configuration stability. Trenton configures, integrates and validates this shallow-depth, high-performance computer ahead of time with long-life processors installed on Trenton's JXT6966 single board computer. The system features the BPC7041 PCI Express 2.0 backplane plus multiple storage options. The TCS4500 enables faster system deployments in many diverse applications such as shipboard navigation and submarine communications. Up to four, front access, hot swap 2.5-inch storage drives are provided. The shallow-depth design of the TCS4500 chassis plus the high-performance computing capability of the system's SBC, backplane and storage options creates an industrial server platform that is ideal for space-constrained applications.



Trenton Systems, Gainesville, GA. (770) 287-3100. [www.TrentonTechnology.com].

1U Networking Platform Supports Core2 Processors

A 1U rackmount platform is designed to support network services with flexible processor choices. Built with Intel Embedded IA components to enable OEM product longevity, the PL-80230 from Win Enterprises offers a choice of Intel Core2 Duo, Core2 Quad or more economical Pentium and Celeron processors. Two unbuffered and

non-ECC DDR3 800/1066 MHz DIMM sockets provide memory to 4 Gbytes. The unit features a 3.5-inch SATA HDD and CompactFlash.



In addition to PCI

Express x8, the PL-80230 also supports one mini PCI socket and one PCI expansion slot.

The platform has 6 GbE LAN ports, which is expandable to a maximum of 14 GbE Ethernet ports all available on the front panel. The device also features dual USB 2.0 ports, one RJ-45 console port and LED indicators that monitor power and storage device activities. The PL-80230 is RoHS, FCC and CE compliant. The unit is RoHS compliant and OEM customizations can include logos, unique chassis color and bezel design. PL-80230 units are available now for evaluation and begin selling at \$554 in OEM quantities. Linux (Fedora, MontaVista, SUSE), Microsoft Windows Embedded, Microsoft Windows XP and Microsoft Windows CE 6.0 are supported.

WIN Enterprises, North Andover, MA. (978) 688-2000.

[www.win-ent.com].

Rugged EPIC SBC with Dual-Core Atom and Video Decoder

A rugged EPIC single board computer integrates a dual- or single-core Atom Processor with ICH8M chipset, onboard SSD, H.264 hardware video decoder, networking and robust I/O in a small form factor. It is suitable for applications in harsh environments that require high-end video performance such as vehicle computing platforms, self-service kiosks, digital signage and video surveillance. The ReadyBoard 740 from Adlink Technology features a 1.66 GHz dual-core Intel Atom D510 or single-core Atom D410, one SO-DIMM for up to 2 Gbytes of 667 MHz DDR2 RAM, and a Broadcom Crystal HD H.264 video decoder. Graphics capabilities of the ReadyBoard 740 include VGA, LVDS, DVI output and efficient high-definition playback (1920 x 1080).



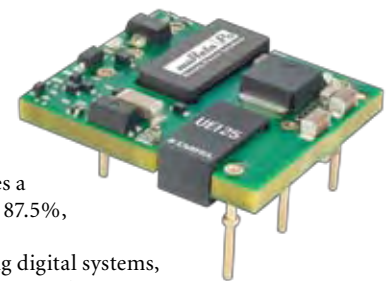
Conducted transient emissions and immunity are well known critical phenomena for power supply in vehicular applications and other severe environments. The MiniModule PWR, an optional power protection module, allows the ReadyBoard 740 to meet the specific demands of in-vehicle power environments. With the MiniModule PWR, the ReadyBoard 740 supports a wide input voltage range, reverse battery protection, overvoltage protection (OVP) and DC/DC converter, making the ReadyBoard 740 an ideal solution for in-vehicle devices. The single unit list price starts at \$410.

ADLINK Technology, San Jose, CA. (408) 495-5557. [www.adlinktech.com].

Low-Profile Open-Frame DC-DC Converters Deliver 25W

One of the biggest design trends in today's military electronics industry is toward reducing size, weight and power (SWaP) in system designs. Power supply technologies are integral to those efforts. Murata Power Solutions has introduced the UEI25-120-D48 series of 25W output, 2:1 input range, 12V output, high-efficiency, isolated DC-DC converters. Featuring 25W output in one square inch of board area, the UEI25-120-D48 series offers efficient regulated DC power for PCB mounting. The low-profile 24.38 x 27.94 x 8.13 mm converters accept a 2:1 input voltage range of 36 to 75 VDC, ideal for telecom equipment. The series also features a 12V output that can be trimmed up or down by 10% with an external trim resistor, plus high efficiency of up to 87.5%, ensuring minimal heat buildup and allowing "no-fan" operation.

These DC-DC converters include full magnetic isolation with Basic insulation, up to 2250 VDC. For powering digital systems, the outputs offer fast settling to step transients and will accept higher capacitive loads. Excellent ripple and noise specifications assure compatibility to noise-susceptible circuits. For systems requiring controlled startup/shutdown and external remote on/off control may use a switch, transistor or digital logic. A wealth of self-protection features avoid both converter and external circuit fails. These include input undervoltage lockout and overtemperature shutdown. The outputs current limit using the "hiccup" autorestart technique and the outputs are short-circuit protected. Additional features include output overvoltage and reverse conduction elimination. It operates in the industrial temperature range of -40° to +85°C.



Murata Power Solutions, Mansfield, MA. (508) 339-3000. [www.murata-ps.com].



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Rugged 10-Port Gigabit Power-over-Ethernet Switch

Axeon has released its new LNP-1002G Lanolinx Industrial Unmanaged Gigabit Power-over-Ethernet Switch. The LNP-1002G is an unmanaged 10-port Gigabit Industrial Ethernet switch with eight 10/100TX ports and two combo ports. The combo ports can either be 10/100/1000TX or Gigabit fiber using an SFP (Small Form Factor Pluggable) module. This configuration provides the user with the flexibility to use fiber or copper ports for the uplink. Each of the eight 10/100TX ports supports the new 802.3af PoE standard and can provide up to 15 watts at 48 VDC. An Extended Operating Temperature model (LNP-1002G-T), with a temperature range from -40° to 80°C, is also available for extreme temperature applications.

Axeon Technologies, Brea, CA. (714) 671-9000. [www.axeon.com].



ATCA Platform Targets Command and Control Apps

ATCA has secured a solid niche in the military market, particularly for applications that stress high-performance communications and networking. RadiSys has announced the Promentum C2 Server, the industry's first pre-integrated, portable ATCA platform designed to provide the performance and features required for rugged, ground mobile applications in the Mil/Aero industry. The C2 Server leverages LCR Electronics' ruggedized ATCA chassis and Astute Networks' Edge Storage Blades in a rapidly deployable, higher performance platform with a more than 30 percent weight decrease and lower power consumption than current Rack Mount Servers (RMS). RadiSys' C2 Server provides integrated computing, switching and storage in one easy-to-manage platform that scales to meet most environmental and performance challenges presented to the Mil/Aero market.

The C2 Server has been designed to meet the demanding environment requirements of MIL-STD-810 and can quickly be deployed and serviced in the field. The computing modules are certified with VMware ESXi, which allows the use of multiple operating systems for consolidation of application, and the use of VSphere to provide cost-effective fault tolerance for critical applications. This pre-integrated RadiSys platform is based on best-of-breed technologies from three trusted industry experts and allows Mil/Aero contractors to focus primarily on their value-add of software and services, while reducing time-to-market. The pre-integrated C2 Server consists of a Ruggedized 6U 6-slot AC LCR Chassis, two RadiSys Promentum



ATCA-2210 10 Gigabit Ethernet Switch and Control Modules with optional COM Express module, which can support platform management functions, up to four RadiSys Promentum ATCA-4500 series single board computers (SBCs) and Astute Networks' Caspian R1100 Edge Storage Blades. The Promentum C2 Server production shipment is planned for the third quarter of 2010.

RadiSys, Hillsboro, OR. (503) 615-1100. [www.radisys.com].

Quad-Channel DataAcq and Processing Card Does 200 MSPS at 16 Bits

Military radar and communications applications have a seemingly endless appetite when it comes to fast A-to-D conversion. The 71600 from Pentek has four 200 MSPS, 16-bit data acquisition channels that deliver nearly 90 dB of spurious-free dynamic range, allowing users to detect small signals of interest surrounded by large interferers. The channels operate from a common clock that can come from an external source or an onboard, programmable, crystal-controlled oscillator. An external clock can drive the ADCs directly as a sample clock or be used as a phase-lock reference for the internal oscillator. The 71660 also utilizes two sync and two gate/trigger signals for synchronizing data acquisition channels across multiple modules.

Four independent memory banks provide the 71660 with a capacity of up to 2 Gbytes of DDR3 SDRAM for applications requiring deep memory, or up to 32 Mbytes of QDRII+ SRAM for applications requiring fast random access. The memory can also be configured to offer two banks of each type, giving users the flexibility to accommodate complex applications. Built-in functions of the memory controller include multichannel ADC data capture, data streaming and tagging of data streams with metadata packets that include channel ID, sample count and time stamp information. The Virtex-6 FPGA on the 71660 provides customers with a combination of turnkey and custom functionality. Customers can select the specific FPGA device installed, ranging from the lower-cost LX130T to the high-performance SX475T with up to 2016 DSP slices. The native form factor for the 71660 is an XMC module and is also offered in a conduction-cooled version. The Model 71660 pricing starts at \$9,995 depending on the memory and FPGA configuration.

Pentek, Upper Saddle River, NJ. (201) 818-5900. [www.pentek.com].



Toolset Aids Design and Deployment of GUIs on Embedded Systems

Created by Blue Water Embedded, Prism is a complete framework and toolset for designing and deploying advanced graphical interfaces on embedded systems, providing everything a developer needs to make UI visions a reality. The Prism Runtime Framework incorporates a complete high-performance graphical drawing library and GUI widget set. This framework provides all of the necessary nuts and bolts to enable users to display professional quality graphics on nearly any target system capable of graphical output. It allows users to incorporate any number of fonts, images, strings and other assets seamlessly on your embedded target, with or without a file system. Developers can easily add their own custom widgets to the framework. Any combination of input devices including keypad, keyboard, touch screen, mouse and multi-touch capable input devices can be utilized within this framework.

Blue Water Embedded, Fort Gratiot, MI.
 (810) 987-3002. [www.bwembedded.com].



DATA STORAGE TECHNOLOGY

RPC12 Ruggedized 3U Fibre Channel RAID System

Phoenix International designs and builds rugged COTS Data Storage Systems that plug and play in any application -- from Multi-Terabyte Fibre Channel RAID and Storage Area Network configurations to plug-in Solid State Disk Drive VME Storage Modules.



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We Put the State of the Art to Work



Low Operational Temperature -20° C

High Operational Temperature +60° C

Operational Altitude to 45,000 feet

8.8 Pound ½ ATR System Suits SWaP Requirements

An 8.8 pound sub-½ ATR, forced air-cooled enclosure for conduction-cooled modules is designed to reduce the Size, Weight and Power (SWaP) of deployed military systems. A fully populated XPand4200 from Extreme Engineering Solutions weighs less than 15 pounds and is suitable for C4ISR applications in vehicles such as UAVs, helicopters, planes, tanks



and light armored vehicles, HMMWVs and UGVs. The XPand4200 conducts heat from conduction-cooled modules to heat exchangers, where the

heat is dissipated to the ambient environment by forced air cooling. The system measures 4.88 x 6.0 x 13.5 inches. The XPand4200 has an optional removable memory module attachment that supports the XPort6191 Solid State Disk (SSD) Removable Storage Module, with 64 Gbytes of storage capacity. With the memory module attachment the height increases to 7.62" and the weight to 11.1 pounds. Up to six conduction-cooled, 0.8" pitch 3U VPX, 3U cPCI, or power supply modules can be configured into the XPand4200. Additionally, the XPand4200 can be configured to meet custom I/O requirements with conduction-cooled PMC/XMC modules available from X-ES or third parties.

The XPand4200 supports Gigabit Ethernet, graphics, RS-232/RS-422, MIL-STD-1553, ARINC 429, as well as custom conduction-cooled PMC/XMC I/O through D38999 circular connectors. An optional front-panel USB port provides system monitoring and maintenance capabilities. There are several power supply options, supporting up to 200W from a MIL-STD-704 28V DC or 115V AC input, as well as internal EMI filtering and hold-up for up to 60 ms at 200W.

Extreme Engineering Solutions, Middleton, WI. (608) 833-1155. [www.xes-inc.com].

GigE-based Vision Appliance Supports Multi-Camera Use

Ethernet is being applied to every kind of interconnect need, including military and security vision applications.

A new Gigabit Ethernet (GigE)-ready vision appliance is compatible with the full range of Dalsa Genie and Spyder3 cameras. GEVA, which stands for GigE Vision Appliance from Dalsa, offers a cost-effective and expandable performance platform for a multitude of



vision tasks. The GEVA platform offers cost savings for multi-camera vision applications, such as final inspection of large assemblies. The high-bandwidth GigE camera ports are compatible with a wide range of mono or color, area and line scan GigE cameras, which can be mixed to suit the application need.

Dalsa, Waterloo, Ont. (519) 886-6000. [www.dalsa.com].



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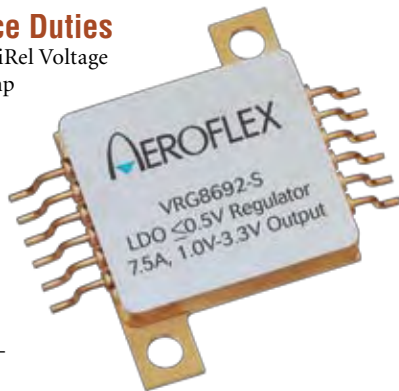
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Hi-Rel Voltage Regulator Ready for Space Duties

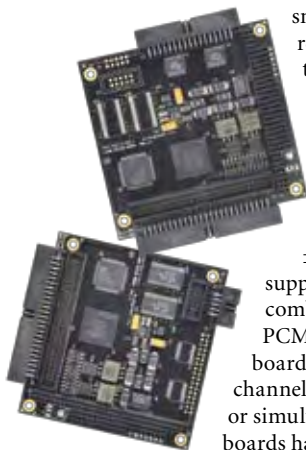
Aeroflex Plainview offers the latest addition to their HiRel Voltage Regulator Family with a new Low Dropout (LDO) 7.5 amp adjustable positive regulator. The VRG8691/92 has an adjustable 1.0V-3.3V output, which uniquely addresses trends in the satellite market requiring lower power supply voltages with higher load currents. The 7.5A VRG8691/92 is a compact, lightweight device ideally suited for supplying power to today's leading FPGA, microprocessor, ASIC and memory chipsets for space applications. The VRG8691/92 includes class K products available to DSCC SMD 5962-09237. The VRG8691/92 is \$4,195, QML Class K, in lots of 100. Both Flight and Non-Flight units are readily available.



Aeroflex, Plainview, NY. (516) 694-6700. [www.aeroflex.com].

Extended Temp PC/104 Analog I/O Cards Need No Calibration

Two new, low-cost PC/104-compatible analog I/O cards operate at a temperature range of -40° to +85° without the need for calibration. Introduced by WinSystems, the PCM-MIO-G-AD-1 is a 16-channel, 16-bit analog input card and the PCM-MIO-G-DA-1 is an 8-channel, 12-bit analog output card. Both cards also support 48 lines of digital I/O. These small, 90 x 96 mm expansion boards are designed to meet customer requirements for accurate analog and digital I/O over an extended temperature range. They are designed for industrial, medical, security, transportation and Mil/COTS applications. Based upon Linear Technologies' precision converters and voltage references, these cards do not require calibration, which results in quick, easy setup; plus it eliminates the necessity for readjustment and recalibration to installed units in the field.



The input ranges for the PCM-MIO-G-AD-1 are 0-5V, $\pm 5V$, 0-10V and $\pm 10V$. Two independent, 16-bit A/D converters support up to 16 single-ended or 8 differential channels or various combinations of both. The conversion speed is 100K samples/sec. The PCM-MIO-G-DA-1 has eight independent, 12-bit D/A converters on board. The output voltage ranges are 0-5V, 0-10V, 5V and 10V. All output channels are programmable and can be updated and cleared individually or simultaneously. Both the PCM-MIO-G-AD-1 and PCM-MIO-G-DA-1 boards have 48 lines of digital I/O individually programmable for input, output, or output with read-back. The lines are TTL-compatible and can

sink 12 mA, which supports direct connection to industry-standard, optically isolated AC and DC signal conditioners. Isolated signal conditioners protect, filter and isolate the analog input and output signals from electrical transients. Both cards are supplied with free drivers for C, Linux and Windows XP Embedded, which can be downloaded free of charge from the website. The PCM-MIO-G-AD-1 list price is \$249 and the PCM-MIO-G-DA-1 list price is \$279.

WinSystems, Arlington, TX. (817) 274-7553. [www.winsystems.com].

SBC Brings Core i7 Performance to 6U cPCI

A 6U CompactPCI SBC is based on the latest Intel Core i7 mobile processor technology. The CO6002 from Kontron sports a 2.53 GHz Intel Core i7-610E or the LV 2.0 GHz Intel Core i7-620LE. On the memory side, up to 8 Gbytes of soldered DDR3 1066 MHz ECC memory ensures data accuracy for demanding and safety-critical applications like radar, sonar, or imaging systems. In addition to the CompactFlash socket for rugged, industrial grade flash modules, up to 32 Gbytes of NAND flash are possible via SATA interface, which are able to hold complete operating systems or application code, substantially increasing overall system speed and availability. The Kontron CP6002 is offered in three versions, with either one (CP6002-R1) or two XMCs/PMCs slots (CP6002-R1-MC and CP6002-R2-MC).

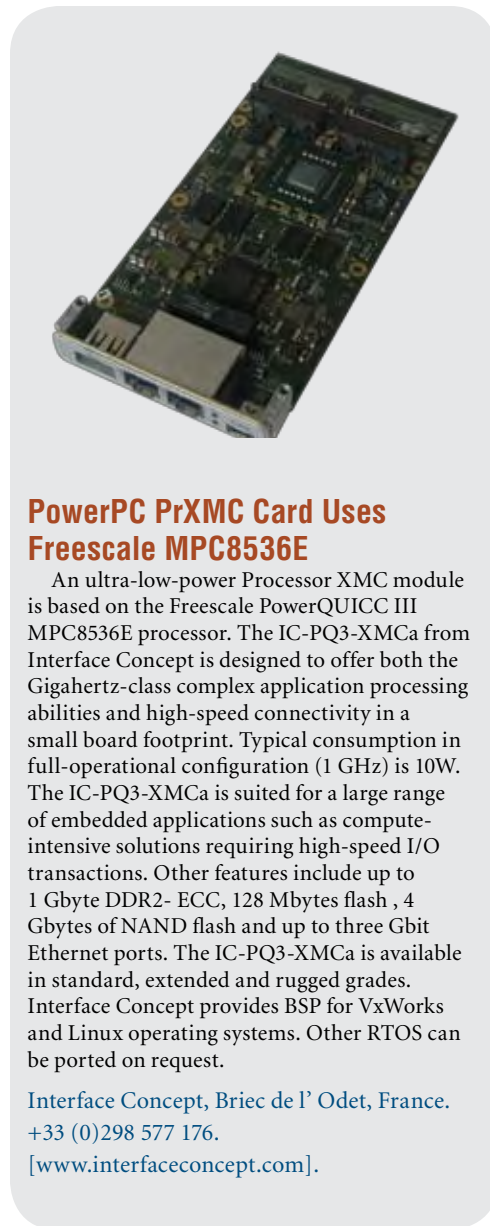
Kontron, Poway, CA. (888) 294-4558. [www.kontron.com].



PowerPC PrXMC Card Uses Freescale MPC8536E

An ultra-low-power Processor XMC module is based on the Freescale PowerQUICC III MPC8536E processor. The IC-PQ3-XMCA from Interface Concept is designed to offer both the Gigahertz-class complex application processing abilities and high-speed connectivity in a small board footprint. Typical consumption in full-operational configuration (1 GHz) is 10W. The IC-PQ3-XMCA is suited for a large range of embedded applications such as compute-intensive solutions requiring high-speed I/O transactions. Other features include up to 1 Gbyte DDR2- ECC, 128 Mbytes flash, 4 Gbytes of NAND flash and up to three Gbit Ethernet ports. The IC-PQ3-XMCA is available in standard, extended and rugged grades. Interface Concept provides BSP for VxWorks and Linux operating systems. Other RTOS can be ported on request.

Interface Concept, Briec de l' Odet, France.
 +33 (0)298 577 176.
 [www.interfaceconcept.com].





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Fanless Panel PCs Balance Performance and Power Consumption

Two new fanless panel PCs are powered by Intel Atom N270 processors. The PPC-L128T and PPC-L157T from Advantech are 12.1" and 15" fanless panel PCs that deliver high performance while consuming low power. They operate with low noise levels and provide display



resolutions up to 1024 x 768 (XGA) pixels. The PPC-L128T and PPC-L157T PCs are both equipped with dual Gigabit Ethernet connectors that support either failover or LAN teaming. The PPC-L128T optionally supports a sunlight-readable display, making it suitable for outdoor use. The PPC-L128T and PPC-L157T are designed with the Atom 1.6 GHz N270 processor combined with 945GSE + ICH7M chipsets. The chipsets are rated at 2.5W, 4W and

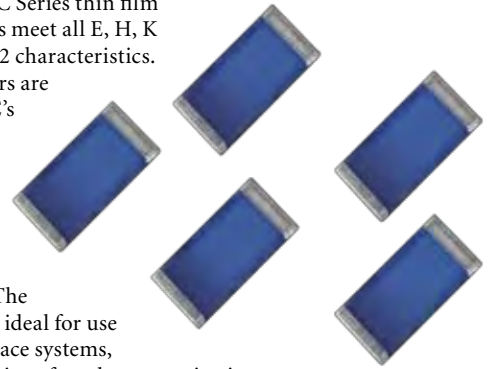
1.5W respectively. The system's fanless design provides passive cooling, and its low noise operation makes the PPC-L128T and PPC-L157T suitable for many environments.

Advantech, Irvine, CA. (800) 866-6008. [www.advantech.com].

Precision Thin Film Chip Resistors Meet MIL-PRF-55342 Specs

TT Electronics IRC has expanded its family of military-qualified thin film chip resistors. The PFC Series precision chip resistors now include a 0402 package size qualified to MIL-PRF-55342 specifications. The PFC Series thin film precision chip resistors meet all E, H, K and M MIL-PRF-55342 characteristics.

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TT Electronics IRC, Corpus Christi, TX. (361) 992-7900.
[\[www.ttelectronics-na.com\]](http://www.ttelectronics-na.com).

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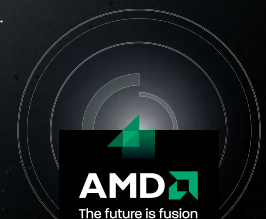
¹ As of June 23, 2010, AMD Opteron 4100 Model 41GL EE (8x 40W 1.8GHz) compared to Intel L5638 (6-core 2.0GHz) (60W)

² Internal testing of AMD Opteron 4100 Model 41GLEE (8x 40W 1.8GHz) versus published results of AMD Opteron 2300 Model 23KS (4x 50W 2GHz)

³ AMD Opteron 4100 Processor 2-channel DDR3-1333 vs AMD Opteron 2300 series 2 channel DDR2-800

⁴ AMD Opteron 4100 Processor HT3 6400MT/s (25.6GB/s) vs AMD Opteron 2300 HT3 4800MT/s (19.2GB/s)

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Special Feature: Multifunction Boards Combine I/O Forces Thanks to the magic of today's level of semiconductor integration, multifunction mezzanine products have emerged enabling military system designers to blend a variety of I/O functions onto a single PMC, XMC or AMC mezzanine card. This section surveys the available products mixing multiple channels of 1553, ARINC-429, Serial I/O and other interfaces on one card. We'll also examine how those multifunction I/O cards are being using in military ground, airborne and shipboard applications.

Tech Recon: Power Issues in Box-Level Systems There's no avoiding the trend toward processors and other key components ramping up in wattage. And more power means more challenges in dissipating heat. Rugged box-level systems are now available that address these problems themselves. Exotic techniques such as spray-cooling and liquid-cooling are all on the table as possible ways to attack the cooling challenge. Articles in this section touch on all these present-day and future cooling solutions.

System Development: Modular Desktop Hardware in Military Test & Instrumentation Fading fast are the days when complex military electronics systems required large racks on boards to implement test platforms for them. Now the same test functions can be done on the PC using USB, PCI Express data acquisition and test modules. This section looks at the boards and software solutions driving this trend.

Tech Focus: Small Form Factor Boards While standard, open-architecture board form factors continue to dominate in military systems, non-standard form factors free designers from the size and cost overheads associated with including a standard bus. Articles in this section look at the trade-offs between standard and non-standard form factors. A product album compares the latest representative of small non-standard boards.



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Editorial

Jeff Child, Editor-in-Chief

Another Season, Another Panel

As sure as the seasons come and go, the defense industry can't go more than five years without taking another crack at that beast called acquisition reform. Numerous panels have studied the acquisition process in the past 25 years, and there has not been a lot of evidence of improvement. Lofty panel and committee discussions on Defense Acquisition Policy reform have been popping up starting as far back as 1986 and the David Packard commission. A more recent example is the Defense Acquisition Performance Assessment (DAPA) committee, which came about in the summer of 2005. DAPA marked the beginnings of then Deputy Defense Secretary Gordon England's efforts to transition to a "simplified" acquisition process and to restore confidence in the acquisition system. Time for another panel.

It's good that serious efforts are being made to tackle acquisition reform. The ongoing problem of military programs going over budget and off schedule hasn't shown any signs of going away. A GAO report in May confirmed that, in aggregate, cost and schedule growth in the DoD's portfolio of major defense acquisition programs continues. What the report also discovered, however, is that individual programs vary greatly in terms of cost growth and schedule delays. Its analysis of individual program performance identified that 21 percent of programs appear to be stable and on track with original cost and schedule goals. Interestingly, those programs were mostly newer ones and had development cycles that were shorter.

The GAO did a series of case studies on some of these example "stable" defense programs. A couple Air Force success stories include the Small Diameter Bomb (SDB) and the Joint Direct Attack Munition (JDAM) programs. The SDB program actually reduced development costs by almost 5 percent and unit costs by more than 14 percent. The system was even available one month earlier than scheduled. Meanwhile, the JDAM program reduced unit costs by 25 percent, which helped enable the Air Force to purchase more than twice the number of units originally planned.

The GAO study cited two Navy programs—Standard Missile-6 (SM-6) Extended Range Active Missile and the P-8A Multi-mission Maritime Aircraft—in their case study analyses. The SM-6 program was on track to reduce expected development costs by more than 7 percent and unit costs by almost 4 percent, and expected to deliver initial capability on schedule. And the P-8A was on track to reduce estimated development costs by almost 4 percent with less than 1 percent increase in unit cost, and was scheduled to

deliver initial capability on time. The Army, for its part, had a vivid example of success with its High Mobility Artillery Rocket System (HIMARS). HIMARS delivered initial capability on time in 2005. And even though development costs for the program grew about 20 percent from original estimates, that increase mostly reflects a requirement that came later to up-armor the vehicle in response to new threats in the wars in Iraq and Afghanistan.

Fast forward to this year, and the latest incarnation of "panel-dom" comes from Congress this time. The Panel on Defense Acquisition Reform was appointed in March 2009 to carry out a comprehensive review of the defense acquisition system. The panel approved its interim report in March of this year, and in summary, it found that while the nature of defense acquisition has substantially changed, the defense acquisition system has not kept pace.

While a lot of the material in the panel's report spoke in terms of generalities, there were a couple insights that made me sit up and take notice. The report said that "...while the Department is currently working to modernize in the 'information age', the acquisition system is particularly poorly designed for the acquisition of information technology." I'm always on the lookout for mentions of embedded computing and software functionality and so forth. An awareness of those critical parts of modern weapons systems is often glossed over in many high-level discussions. Information Technology (IT) is a term that in these contexts sometimes lumps in all types of computing—which can be misleading.

A table in the report illustrated the trend that's crept up on the industry, whereby the main theme of system design today is for the great majority of functionality to be implemented as software running on an embedded computer. In the F-111 aircraft of 1970, only 20 percent of its system functionally was implemented as software running on embedded computers. The F-16 (circa 1982) ran around 45 percent of its functions, and for the F-22 that grew to 80 percent. In short, the percentage of functionality provided by software has increased tenfold over the past 40 years. The report cites that "... as software and IT are becoming more prevalent in weapon systems, the complexity of these systems is growing exponentially." The "IT" they're referring to is embedded computers obviously. The good news—even though you'll never see it mentioned explicitly in these kinds of panels discussions—is that making maximum use of the embedded computing products and expertise of our industry are and will continue to be helpful for reducing costs and development times for today's complex military systems. ■■



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